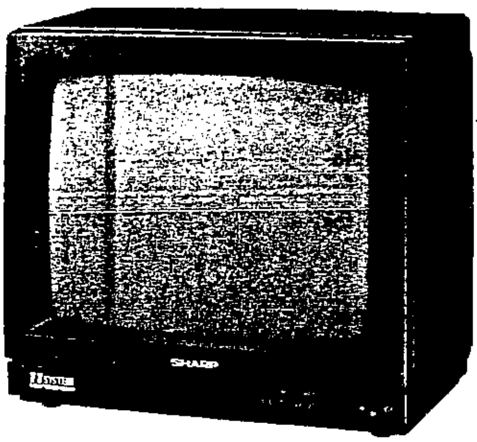
SHARP SERVICE MANUAL

S86H9C1410SPN

6P-M CHASSIS

11 SYSTEM COLOUR TELEVISION



MODEL DV-1410SPN

In the interests of user-safety (Required by safety regulations in some countries) the set should be restored to its original condition and only parts identical to those specified should be used.

CONTENTS

ELECTRICAL SPECIFICATIONS

Aerial Input Impedance .... 75 ohm unbalanced
Convergence .... Self Converging System
Focus .... Bi-potential, Uni-potential electrostatic
Audio Power Output Rating .... 2W (MAX)
Intermediate Frequencies
  Picture IF Carrier Frequency .... 38.9 MHz
  Sound IF Carrier Frequency .... 32.4 MHz (6.5 MHz)
    32.9 MHz (6.0 MHz)
    33.4 MHz (5.5 MHz)
    34.4 MHz (4.5 MHz)
Colour Sub-Carrier Frequency .... 34.47 MHz (PAL/NTSC)
  34.494/34.65 MHz (SECAM)
  35.32 MHz (NTSC)
Power Input .... AC 110/127/220/240 Volts
  50 Hz/60 Hz (Auto)
Power Consumption .... 69 Watt
Speaker Size .... 8 cm (8 ohm)
Sweep Deflection .... Magnetic

RECEIVING CHANNELS
  PAL-B/G, SECAM-B/G .... VHF: E2~E12 ch
    CATV: S1~S3, M1~M10, U1~U10 ch
    UHF: 21~69 ch
  PAL-D/K, SECAM-D/K .... VHF: R1~R12 ch
    UHF: 21~69 ch
  PAL-I .... VHF: B~J ch (Ireland)
    UHF: 21~69 ch (U.K., H.K.)
  NTSC-M .... VHF: US;2~13 ch JAPAN;1~12 ch
    CATV: A-6~A-1, A~W, AA ch
    UHF: US;14~83 ch JAPAN;13~62 ch

RECEIVING FREQUENCY
  VHF: 48.25~301.25 MHz
  UHF: 471.25~885.25 MHz

WARNING

The chassis in this receiver is partially hot. Use an isolation transformer between the line cord plug and power receptacle, when servicing this chassis.
To prevent electric shock, do not remove cover. No user — serviceable parts inside. Refer servicing to qualified service personnel.

SHARP CORPORATION

IMPORTANT SERVICE NOTES

Maintenance and repair of this receiver should be done by qualified service personnel only.

SERVICING OF HIGH VOLTAGE SYSTEM AND PICTURE TUBE

When servicing the high voltage system, remove static charge from it by connecting a 10k ohm Resistor in series with an insulated wire (such as a test probe) between picture tube tag and 2nd anode lead. (AC line cord should be disconnected from AC outlet.)

1. Picture tube in this receiver employs integral implosion protection.
2. Replace with tube of the same type number for continued safety.
3. Do not lift picture tube by the neck.
4. Handle the picture tube only when wearing shatter-proof goggles and after discharging the high voltage completely.

X-RAY

This receiver is designed so that any X-ray radiation is kept to an absolute minimum. Since certain malfunctions or servicing may produce potentially hazardous radiation with prolonged exposure at close range, the following precautions should be observed:

1. When repairing the circuit, be sure not to increase the high voltage to more than 30.0 kV, (at beam 0μA) for the set.
2. To keep the set in a normal operation, be sure to make it function on 21.75 kV ± 1.5 kV (at beam 800μA) in the case of the set. The set has been factory-adjusted to the above-mentioned high voltage.

   ∴ If there is a possibility that the high voltage fluctuates as a result of the repairs, never forget to check for such high voltage after the work.
3. Do not substitute a picture tube with unauthorized types and/or brands which may cause excess X-ray radiation.

BEFORE RETURNING THE RECEIVER

Before returning the receiver to the user, perform the following safety checks.

1. Inspect all lead dress to make certain that leads are not pinched or that hardware is not lodged between the chassis and other metal parts in the receiver.
2. Inspect all protective devices such as non-metallic control knobs, insulating fishpapers, cabinet backs, adjustment and compartment covers or shields, isolation resistor-capacity networks, mechanical insulators etc.

DESCRIPTION OF NEW CIRCUIT

OPERATION DESCRIPTION ON MICROPROCESSOR
RH-IX0761CEZZ

The microprocessor IX0761CE is used for the operations of this model, such as tuning, channel selection, sound volume control, remote control, function processing, CRT display. The following describe the operations of the microprocessor IX0761CE.

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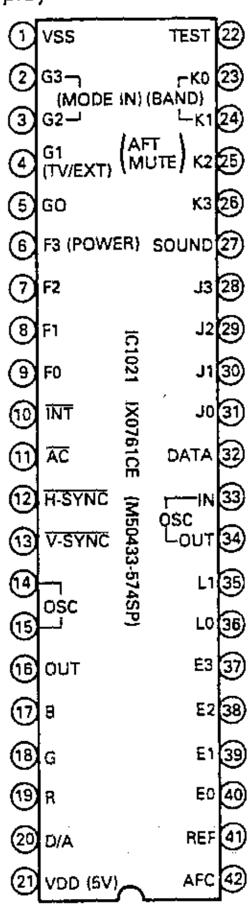


Figure 1. Pin Connections

1. FUNCTIONAL DESCRIPTIONS

1-1. Key Matrix

Table 1. Key Matrix Arrangement

	L_1	L_0	J_0	J_1	J_2	J_3
E_3	—	PWR	TU UP	TU DN	VOL UP	VOL DN
E_2	—	TV/AV	FT UP	FT DN	CONT UP	CONT DN
E_1	—	—	CH UP	CH DN	COL UP	COL DN
E_0	—	—	AUTO/ MANUAL	—	—	—

The keys are read at intervals of 40 msec. When a key is pressed for about 40 msec or longer, the key entry is decoded and the command is executed. Entries from the key matrix take precedence over entries from the remote controller.
If two or more keys are pressed simultaneously, neither of their commands entered is not executed. If two or more keys pressed simultaneously are those among the typamatic keys CHUP, CHDN, VOLUP, VOLDN, VTUP and VTDN, the command of the last pressed key is executed. If the keys pressed at the same time are not typamatic keys, neither of these key commands is executed unless a key is newly entered after releasing all the keys.

1-2. Signal Receiption from Remote Controller

When a remote control signal enters the INT input, an interruption is made and control goes to the remote control processing routine so that the microprocessor reads 15-bit data of the foreground signal and then 15 bits of the background signal. It thereafter performs inversion check on the foreground and background signals.
If this remote control signal is valid, the bit data is decoded and the command is executed. However, the command is cancelled unless the same code is received for about 200 msec or longer.

Table 2. Codes and Commands (Data Consisting of C_0 through C_{15})

No.	C_1 C_2 C_3 C_4 C_5 System Code	C_6 C_7 C_8 C_9 C_{10} C_{11} Data	C_{12} C_{13} Extension	C_{14} Mask	C_{15} K	Command
1	1 0 0 0 0	0 1 1 0 1 0	0 0	1	×	Power ON/OFF
2	1 0 0 0 0	0 0 1 0 1 0	0 0	1	×	VOL UP
3	1 0 0 0 0	1 0 1 0 1 0	0 0	1	×	VOL DOWN
4	1 0 0 0 0	1 1 1 0 1 0	0 0	1	×	MUTE
5	1 0 0 0 0	0 1 0 0 0 1	0 0	1	×	Cont-up
6	1 0 0 0 0	1 1 0 0 0 1	0 0	1	×	Cont-Down
7	1 0 0 0 0	0 0 1 0 0 1	0 0	1	×	Colour-UP
8	1 0 0 0 0	1 0 1 0 0 1	0 0	1	×	Colour-DOWN
9	1 0 0 0 0	1 0 0 0 0 1	0 0	1	×	Cont/colour Normal
10	1 0 0 0 0	1 1 0 1 1 0	0 0	1	×	Call
11	1 0 0 0 0	1 1 0 0 1 0	0 0	1	×	TV/AV
12	1 0 0 0 0	0 1 0 1 1 0	0 0	1	×	OFF TIMER
13	1 0 0 0 0	1 0 0 0 1 0	0 0	1	×	CH-UP
14	1 0 0 0 0	0 1 0 0 1 0	0 0	1	×	CH-ON
15	1 0 0 0 0	0 1 0 1 0 0	0 0	1	×	Pr 0
16	1 0 0 0 0	1 0 0 0 0 0	0 0	1	×	Pr 1
17	1 0 0 0 0	0 1 0 0 0 0	0 0	1	×	Pr 2
18	1 0 0 0 0	1 1 0 0 0 0	0 0	1	×	Pr 3
19	1 0 0 0 0	0 0 1 0 0 0	0 0	1	×	Pr 4
20	1 0 0 0 0	1 0 1 0 0 0	0 0	1	×	Pr 5
21	1 0 0 0 0	0 1 1 0 0 0	0 0	1	×	Pr 6
22	1 0 0 0 0	1 1 1 0 0 0	0 0	1	×	Pr 7
23	1 0 0 0 0	0 0 0 1 0 0	0 0	1	×	Pr 8
24	1 0 0 0 0	1 0 0 1 0 0	0 0	1	×	Pr 9
25	1 0 0 0 0	1 1 1 1 0 1	0 0	1	×	Pr 1*
26	1 0 0 0 0	0 0 0 0 1 1	0 0	1	×	Pr 2*
27	1 0 0 0 0	1 0 0 0 1 1	0 0	1	×	Pr 3*
28	1 0 0 0 0	0 1 1 0 0 1	0 0	1	×	—

1-3. Presetting

Presetting can be searched automatically and manually. The [AUTO/MANUAL] key in the key matrix is used to change the search mode.

[AUTO/MANUAL] key entry becomes valid when the preset switch position is changed from the normal mode to preset mode VHF or UHF. Every time the [AUTO/MANUAL] key is operated, the search mode is changed between AUTO and MANUAL.

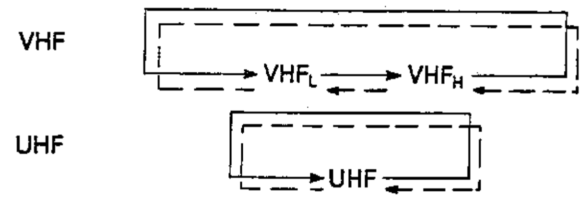
When the preset switch position is changed from the normal mode to the preset mode, the microprocessor is put in AUTO SEARCH mode.

1-3-1. AUTO SEARCH

When the preset switch position is changed from the normal mode to preset-mode VHF or UHF, the microprocessor is put in AUTO SEARCH mode, whereby the AFT-MUTE (K_2) output goes "Low".

When the TUNING [UP] or [DN] key is entered, searching up or down is started. While searching, "High" voltage is outputted from Port F_1, the band display turns red and the AFT-MUTE (K_2) output becomes "High". Upon completion of searching, the AFT-MUTE output and the voltage at Port F_1 go "Low" while the band display turns green.

The turning voltage of any band is changeable.



The tuning voltage is also changeable by operating the FINE [UP] or [DN] key for fine adjustment even in AUTO SEARCH mode, though it is unchangeable while the search is going on. When the search ends or when the FINE [UP] or [DN] key is released, the tuning voltage and band data are written in the address of EAROM that corresponds to the current channel position.

If the preset switch position is changed to the normal mode during the search or if the [POWOFF] or [AUTO/MANUAL] key is entered during searching, the search stops.

1-3-2. MANUAL SEARCH

When the preset switch position is changed from the normal mode to the preset mode (VHF or UHF) and the [AUTO/MANUAL] key is pressed to obtain the MANUAL mode, the AFT-MUTE (K_2) output goes "Low".

The tuning voltage of any band is changeable by entering the TUNING [UP] or [DN] or FINE [UP] or [DN] key. When the TUNING [UP] or [DN] key is pressed, the tuning voltage goes up or down fast for coarse adjustment. When the FINE [UP] or [DN] key is used, the tuning voltage goes up or down slowly for fine adjustment.

When the TUNING [UP] or [DN] or FINE [UP] or [DN] key is released, the tuning voltage and band data are written in the address of EAROM which corresponds to the current channel position.

Channel selecting operation in preset mode does not perform channel selection but only changes the channel position display on the screen.

Table 3. Band Outputs

	K_1	K_0
VHF_L	L	L
VHF_H	L	H
UHF	H	L

1-4. Channel Selection

Up to 19 channels can sequentially be selected by the use of the [CH UP] or [CH DN] key of the key matrix or remote controller. While the key is kept pressed, the channel positions are changed every 0.7 second. The channels can also be selected directly by the remote controller (Two actions are required for selection of a channel whose No. is 10 or larger).
If the command is entered to select the same channel position as the channel position currently on, no channel selecting operation is performed but only its channel position is displayed.
When channel selection is performed, the VT, band and AFT data stored in the EAROM address corresponding to the channel position now selected are read and set. If the AFT data is off, the AFT-MUTE output (K_2) remains "Low" even after channel selecting operation is performed.
The 2-digit channel selection mode is obtained by operating the "Pro 1*" key. The channel position display thereby appears as "1-". When one of the keys from Pro 0" through "Pro 9" is pressed within about 6 seconds after pressing "Pro 1*" key, the channel is selected.

1-5. Sound Volume

PWM clock which is changeable in 64 steps is outputted from the sound volume control output VDP (at intervals of about 1 msec). The VDP output is changeable by the use of the [VOL UP] or [VOL DN] key of the key matrix or remote controller (The MUTE function is available only by the remote controller).
With the [VOL UP] or [VOL DN] key pressed, approximately 8 seconds are needed to change the volume from the minimum (or maximum) to the maximum (or minimum). (The sound volume display appears simultaneously with the key entry, and disappears about 3 seconds after the key is released.) When the volume reaches its maximum or minimum, it stops changing at that point.
The polarity of the VDP output goes "Low" when the VDP output reaches the minimum or when the MUTE function is turned ON.
When the [MUTE] key is pressed in MUTE OFF state, the MUTE function is turned ON and the VDP output becomes minimum. When the [VOL UP], [VOL DN] or [MUTE] key is pressed in MUTE ON mode, the MUTE function is turned OFF.
When the [VOL UP] or [VOL DN] key is released, the analog quantity at that point is written into EAROM. The previous state is read after the auto clear is cancelled.

1-6. Contrast and Colour Control by DAC

The DA converter IC IX0762CE (IC1025) is used to input the output control signal from Pin ⑮ (F2) and Pin ㉘ (J3) to the Pin ⑨ (FO), Pin ⑯ (S) and Pin ⑩ (F1) so that the contrast and colour outputs are controlled.

Table 4.

	IX0762CE
Contrast output	Pin ⑰ (D_0)
Colour output	Pin ⑱ (D_1)

When the "CONT UP/DN" or "COLOUR UP/DN" key of the key matrix or remote controller is entered, the analog quantity concerned is increased or decreased. The porality goes "Low" when minimum, and goes "High" when maximum.
When the CONT/COLOUR-NORMAL keys of the remote controller is pressed, the CONT output is normalized to 2/3 and the COLOUR output to 1/2, and these data are written into EAROM.
When the CONT/COLOUR UP/DN key is released, the data of the CONT or COLOUR output is written into EAROM.

1-7. POWER ON/OFF

The POW key is a toggle key. The power control output F_3 is changed every time this key is entered.
When the power is turned on, the output F_3 goes "High" and the channel which was on before the power was previously turned off is selected. Also, the MUTE state is cancelled and the previous output state is resumed.
When the power is turned off, the output F_3 goes "Low", the analog control output VDP "Low", and the D/A output "High".
When the power is off, only POW key entry is effective and no other key entry is not accepted.

1-8. FT(+) and FT(−) keys (in Normal Mode)

The FT(+) and FT(−) keys are effective in both normal and preset modes. These keys are used to fine adjust the tuning voltage on a bit-by-bit basis.
When the tuning voltage reaches its maximum or minimum, the tuning operation stops at that point. When the FT(+) or FT(−) key is released, the tuning voltage, band and AFT data obtained at that point are written in the address of EAROM which corresponds to the current channel position.
If the key is pressed in normal mode, the output at the AFT pin goes down to the "Low" level and the CH sign No. is displayed in yellow (for 3 seconds if not in CALL mode).

1-9. MUTE Key

Operating the MUTE key of the remote controller alternately changes the volume output VDPO between the MUTE state (the output always at "Low" level) and the previous non-MUTE state. This key entry is acceptable in both normal and preset modes.
MUTE display on the CRT is as follows:

- In preset mode
  MUTE display remains for 3 seconds after the key is released, followed by the preset display. The key entry is not accepted during the search.
- In normal mode
  MUTE display continues ON after the key is released. If any other key is pressed and display of that key entry thereby appears, MUTE display resumes after 3-second display of that key entry.

1-10. Colour System Display Control

Colour system display corresponds to the display switching inputs G_2 and G_3 as follows:

Table 5.

Display Switching Input		System Display					
G_2	G_3	Display Character	Display Colour	P	G	B	OUT
Pin ⑲	Pin ⑳	—	—	Pin ③	Pin ④	Pin ⑤	Pin ⑥
L	L	—	—	—	—	—	—
L	H	PAL	yellow	○	○	—	○
H	L	SECAM	red	○	—	—	○
H	H	NTSC	green	—	○	—	○

1-11. Off-Timer

Up to 120-second off-timer setting can be achieved by operating the [OFF-TIMER] key of the remote controller. The setting time is decreased by 30 seconds with a single entry of the key.

Off-timer cancelled → 120 sec. → 90 sec. → 60 sec. → 30 sec. →

The off-timer is set (or cancelled) every time the [OFF-TIMER] key is pressed, as shown above.
When the microprocessor is put in preset mode while the off-timer is in operation, the off-timer operation is cleared. In preset mode, the off-timer cannot be set. The timer starts operation when it is set.
Turning off the power during off-timer operation cancels it.

1-12. Program Call

The program call is a toggle command which is available with operation of the CALL key of the remote control. Each time the CALL key is pushed, the display on CRT is changed one after another as follows:

- Without the off timer turned on:

Display OFF mode
↓
Display ON (Large) mode
↓
Display ON (Small) mode
↓

- With the off timer turned on:

Display OFF mode
↓
Timer residual time display mode
↓
Display ON (Large) mode
↓
Display ON (Small) mode
↓

1-13. TV/AV mode selection

The TV and AV modes can be selected through the key matrix or remote-control transmitter. This mode selection is accomplished according to the toggle command. The TV/AV mode selector switch alternately selects the TV or AV mode as follows.

→ G1="L" (TV mode) → G1="H" (AV mode) →

This switch is also used as the AUTO/MANUAL SEARCH mode selector switch; and it can achieve the TV/AV mode selection when the preset mode switch is in the NORMAL position. (When the preset mode switch is in the VHF or UHF position, it can accomplish the AUTO/MANUAL SEARCH mode selection.)

Preset mode switch position	Mode select operation
NORM	TV/AV
VHF	AUTO/MANUAL SEARCH
UHF	AUTO/MANUAL SEARCH

<Changeover between TV/AV mode selection and AUTO/MANUAL SEARCH mode selection>
When the preset mode switch (SW3) is set to the NORMAL position, the base voltage of Q3 reaches 0V to turn it off. As a result, a bias is applied from +B (12V) to the base of Q1 to turn it on, enabling the TV/AV mode switch (SW1). At this time the AUTO/MANUAL mode switch (SW2) is disabled because Q2 is in the OFF state.
When the preset mode switch (SW3) is in the VHF or UHV position, a pulse voltage is applied through this switch, which causes a voltage integrated by R3, R4, and C1 to be applied to the base of Q3, resulting in Q3 being turned on. As a result, Q1 is put in the OFF state to disable SW1 and Q2 is put in the ON state to enable SW2. This means that the TV/AV mode selection can occur when the preset mode switch is in the NORMAL position and that the AUTO/MANUAL SEARCH mode selection can occur when the preset mode switch is in the VHF or UHF position.

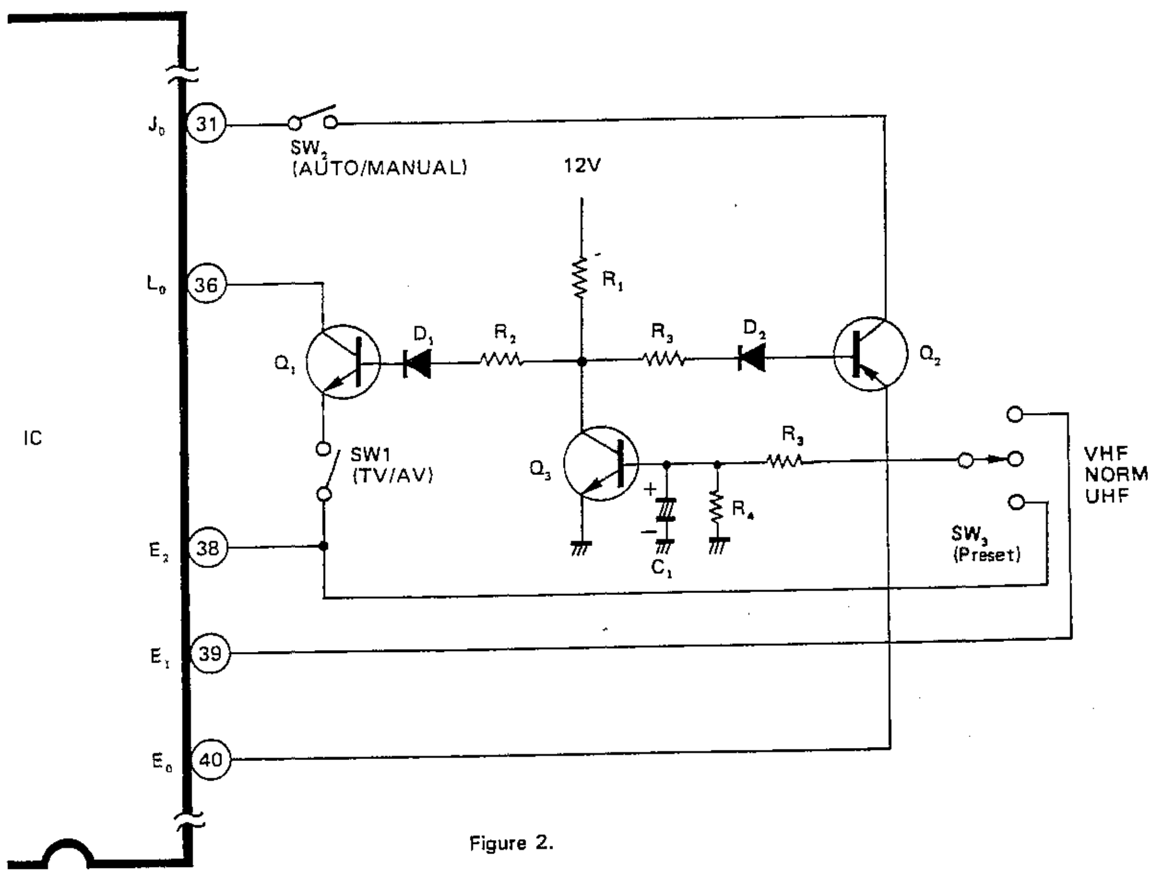
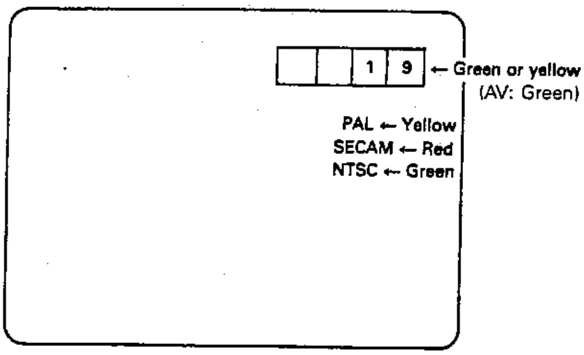


Figure 2.

During the display ON mode, program No. is always indicated on CRT. And during the timer residual time display mode, the residual time continues to be indicated at the intervals of 1 minute.
In other than the timer residual time display mode, the residual time display is carried out at the intervals of about 3 seconds in the unit of 5 minutes, as far as the off timer has been turned on.

2. SCREEN DISPLAY

2-1. Channel Position Display (Large)



10 sec. when power is turned on.
3 sec. in other cases.

Figure 3.

If the set is in the TV mode while in the display or display on mode (this mode is on for about 3 or 10 seconds after the power-on, channel select, or TV/AV select operation is performed), it displays a channel position, and if it is in the AV mode, it displays "AV".
A system display occurs concurrently only when the set is in the large display mode. The colour of the AFT OFF position is yellow.

2-2. Channel Position Display (Small)

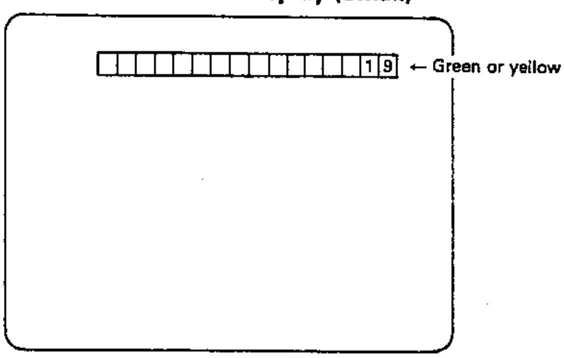


Figure 4.

Set in display (small) mode by the "CALL" key, the channel position (small) is always displayed on the screen.
The position display colour is yellow when AFT is OFF.

2-3. Off Timer Residual Time Display

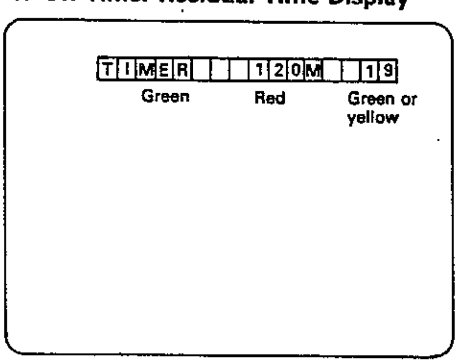


Figure 5.

For about 3 seconds after the OFF TIMER key has been pushed or while the unit is in the off timer residual time display mode, there appears the display on CRT as shown above.
During this mode, the residual time is displayed every 1 minute, and during the other modes, it is displayed for about 3 seconds every 5 minutes.
From the time 5 seconds before the off timer function has been stopped, the sign "OM" starts flashing at the intervals of 1 second. After that, the unit will be turned off.

2-4. Sound Volume Display

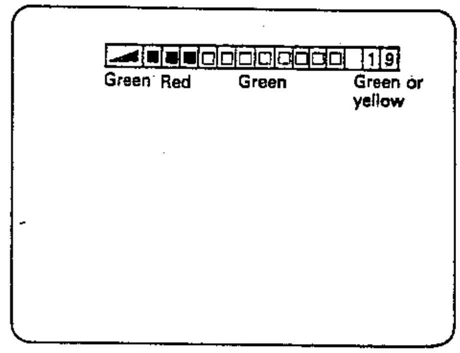


Figure 6.

When the VOL UP or VOL DN key is being pushed and in about 3 seconds after that key has been touched off, there appears the sound volume display on CRT as shown above.
The sound volume is also displayed when the MUTE key is pushed: with the muting turned on, the display appears in the same way as with the sound volume being set at the minimum.

2-5. Preset Display

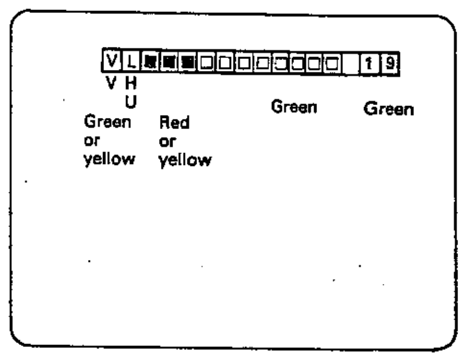


Figure 7.

The data as shown above is always displayed on the CRT screen in preset mode.
The VT data display turns yellow in AUTO SEARCH mode. While searching, the band is displayed in red. It turns green when the search is completed.
The VT data is displayed in red in MANUAL SEARCH mode.

OPERATIONAL DESCRIPTIONS OF DAC RH-IX0762CEZZ

The IC (IX0762CE) is used for controlling the colour and contrast. It controls the two (colour and contrast) DA outputs according to the change of the data inputted from the microprocessor IX0761CE.

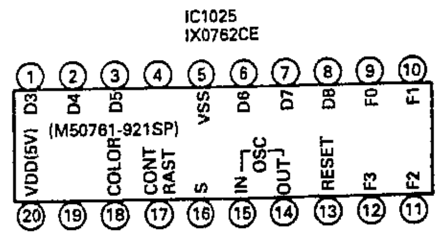


Figure 8. Pin Connection

1. Block Diagram
1-1. Operation of Each Block

2. Functional Description
2-1. Reception Signal
2-2. DAC Output Signal

1. BLOCK DIAGRAM

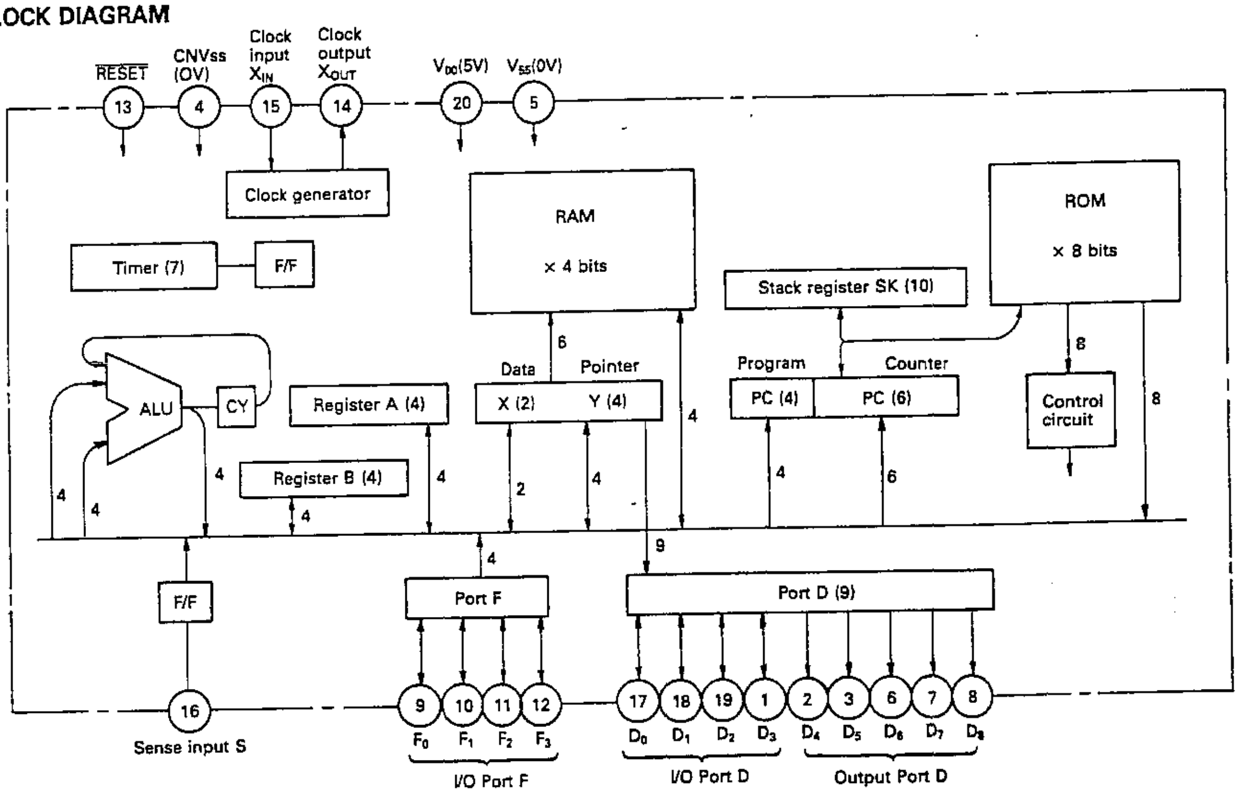


Figure 9. Block Diagram

1-1. Operation of Each Block

Program Memory ROM

A mask ROM whose capacity is 512 characters × 8 bits. User-specified instruction code can be programmed in this ROM.

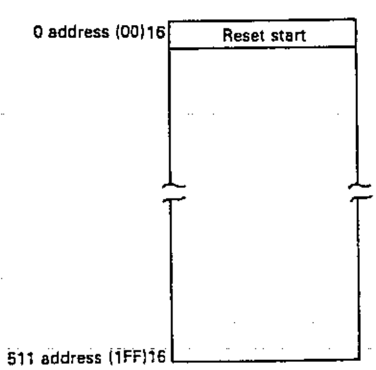


Figure 10. ROM Address Map

Program Counter PC

A counter which specifies the ROM address and determines the sequence of reading the instructions written in the ROM. The program counter (PC) has the capacity of 10 bits and is of polynomible counter type.

p_3	p_2	p_1	p_0	a_5	a_4	a_3	a_2	a_1	a_0

Figure 11. Program Counter

Stack Register SK

A register which, when the subroutine is called, temporarily holds the data, contained in the PC before the subroutine call, until control returns to the original routine.

Data Memory RAM

A storage for various process and control data, having a capacity of 32 characters × 4 bits (128 bits). A character consists of 4 bits, and bit processing is allowed throughout the memory area. Fig. 12 shows the RAM address map.

Y \ X	0				1				2				3			
bit	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
0																
1																
⋮																
6																
7																

Figure 12. RAM Address Map

Data Pointer DP

A register whose function is to specify the RAM address and the bit position of the output port D. The register X consisting of the high-order 2 bits of the DP specifies the RAM file and the register Y consisting of the low-order 4 bits specifies the RAM column.

4 Bit Arithmetic and Logic Unit

A unit whose function is to perform logical operations. It performs addition, subtraction, comparison, and bit processing.

Register A and Carry Flag CY

The register A is an accumulater playing a central part in operation, with the capacity of 4 bits. The carry flag CY stores the carry or borrow from the highest position of the arithmetic and logic unit after various instruction execution. The CY is also usable as a 1-bit flag.

Register B

The register B has the capacity of 4 bits. Used for temporary storage of 4-bit data.

Timer

Consists of a 7-bit counter and associated circuitry. It performs 1/100 division and sets the flag. Restarts counting after setting the flag.
The flag can be tested by the skip command (SNZT).
The timer and the flag are resettable by the system reset and the reset command.

I/O Ports

(1) Port F
Has a function to perform 4-bit output (OFA) and input (IAF). To perform input it is necessary to program the output latch to (1) and to have the output in high impedance state.

(2) Port D
Has functions to perform 9 1-bit outputs (SD, RD) and to perform 4-bit input (IAD). There are 1-bit latches at the output section and the register Y of the data pointer is used for specifying one of the port D pins to perform output.
Pins D_0-D_3 are used to perform 4-bit input.
To perform input, it is necessary to program the D_0-to-D_3 output latches to (1) and to have the output in high impedance state.
The output is N-channel opened drain circuitry.

(3) Port S
A leading edge active sense input pin. When the signal at the S pin changes from "Low" to "High", the flag is set (1). The flag can be tested by the skip command (SNZS). Execution of the skip command resets the flag. System resetting also resets the flag.
The S pin is changeable into the level active input pin by mask option. The flag (S) becomes invalid in this case.
The S pin can be tested by the skip command (SNZS). Skipped when at th "High" level.

Reset Function

When a "Low" level signal of more than 2 machine cycles is applied to the RESET pin, resetting is performed. When a "High" level signal is applied after resetting, the program is run from the address 0.
When resetting is performed:

(1) The program counter is set to the address 0.
(2) The two flags (timer flag and sense input flag) are reset.
(3) The output latch of Port D is set to (1) (in high impedance state).
(4) The output latch of Port F is set to (1) (in high impedance state).

CNVss Pin

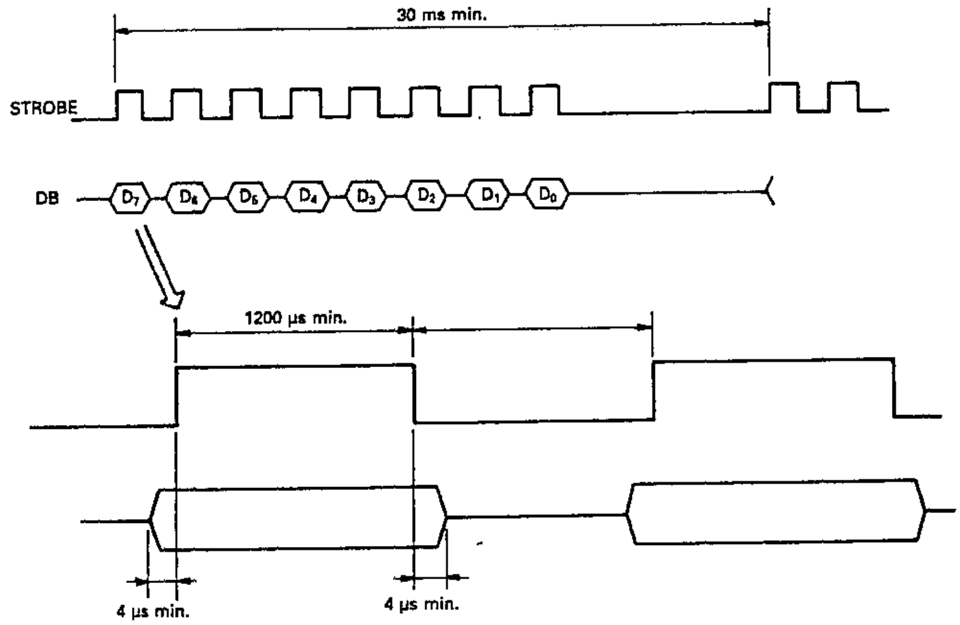
Connect this input to Vss, and be sure to apply the "Low" level input (0 V).

Clock Generation Circuit

The DAC has a built-in clock generator. Provision of an R or ceramic resonator outside the circuit will provide a clock signal. To input the clock signal from outside, connect a clock generating source to the X_{IN} pin and open the X_{OUT} pin.

2. FUNCTIONAL DESCRIPTION

2-1. Reception Signal



Meaning of data

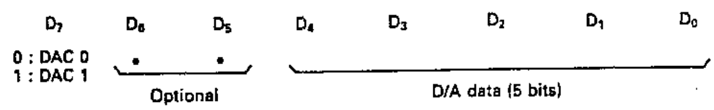


Figure 13.

2-2. DAC Output Signal

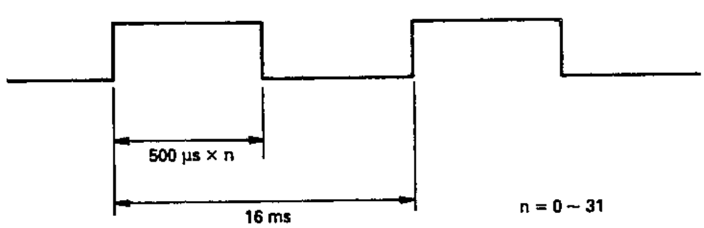


Figure 14.

OPERATIONAL PRINCIPLE OF PAL-VIDEO-CHROMA-JUNGLE LSI (RH-IX0393CEN1)

1. OUTLINE

IC801 (RH-IX0393CEN1) is a chip of video-chroma-jungle LSI, and when combined with IF system IC, it enables colour TV reception. It has a bipolar monolithic structure and is housed in a 48-pin shrink pitch plastic mold DIL. And this IC is further combined with SECAM chroma IC (RH-IX0226CEZZ) to allow TV reception in either of PAL, NTSC and SECAM systems.

2. FUNCTIONS

This IC offers the following functions:

(1) Sync separation
(2) Horizontal AFC
(3) Horizontal oscillation
(4) Vertical oscillation and sawtooth wave generation
(5) Video amplification/control
(6) Chroma amplification/control
(7) ACC/identify/APC detection
(8) VCO (Voltage Control Oscillator)
(9) Chroma demodulation/control

3. FEATURES

(1) The large scale integrated circuit (LSI) results in rationalized design, high reliability and reduced power consumption.
(2) The LSI has electrical performance to meet NTSC system TV as well as PAL system TV.
(3) When combined with SECAM chroma IC (RH-IX0226CEZZ), it can set up a multi TV reception system (PAL/SECAM/NTSC).
(4) Having two different sync inputs (horizontal and vertical), it gives wider achievement in the circuitry design.
(5) In horizontal AFC operation, IF-AGC voltage is used to change AFC time constant in order to reduce horizontal jitters in the weak field; AFC gain is increased to improve the skew distortion when VCR switch is turned on; AFC pull-in range is increased by automatic change of AFC gain based on the sync detector circuit; and audio muting and automatic channel selection are possible.
(6) Vertical drive output is applicable to SRPP output circuit.
(7) There are such output pins as to meet the horizontal sync output (emitter follower), burst gate pulse (emitter follower) and vertical blanking pulse (open collector).
(8) Video DC restoration rate variable pin.
(9) Killer level characteristic in the weak field is improved due to the sync detector system.
(10) High-speed identify operation to meet VCR application.
(11) DC tint control during NTSC reception.
(12) Since the horizontal sawtooth wave is used to produce F/F drive pulse, there is less error of F/F operation even if the flyback pulse becomes abnormal in its waveform.

4. SIGNAL FLOW OF IC801

Fig. 1 is a block diagram of IC801.

The composite video signal which has come from IF circuit via the buffer transistor is applied to the horizontal sync separator input (pin ㉖), vertical sync separator input (pin ㉔), video input (pins ㉗ and ㉘) and chroma input (pin ㉜) after passing through the filter, delay line and other parts respectively.

The signal applied to pin ㉖ is subjected to a horizontal sync separation and goes out of pin ㉕. And it is supplied to the horizontal AFC circuit where it is synchronized with the horizontal oscillation signal, and the resultant signal is sent to pin ⑦; at the same time, BGP (burst gate pulse) is produced from the horizontal sync signal at pin ㉕ and goes out of pin ㊱, and it is also applied to the video/chroma circuit.

The signal applied to pin ㉔ is subjected to a vertical sync separation and is filtered out of pin ㉓, and then it is synchronized with the vertical oscillation signal, and the resultant signal is shaped into a lamp waveform to go out of pin ⑯: at the same time, it is sent to the blanking pulse generator circuit to go out of pin ㉞, and is supplied to the video/chroma circuit.

The video signal applied to pins ㉗ and ㉘ is subjected to an amplification and exeriences controls about its contrast, brightness and tone quality and goes out of pin ⑤.

The chroma signal applied to pin ㉜ is subjected to ACC control and colour saturation control and goes out of pin ㊼. Meanwhile, the burst signal is produced from the chroma signal by sampling of BGP, and is filtered out of pin ㊹ to enter ACC/killer detector circuit, identify detector circuit and APC detector circuit: in the case of NTSC system, the burst signal allows NTSC switch to turn on.

The chroma signal going out of pin ㊼ is sent to pins ㊻ and ㊽ passing through 1H delay line: this applies to the case of PAL system. In the case of NTSC system, the chroma signal is applied directly to pins ㊻ and ㊽. The signals available at pins ㊻ and ㊽ are subjected to R-Y and B-Y demodulations by multiplication with carrier wave from VCO circuit, and go out of pins ① and ② respectively: in the case of NTSC system, the signal experiences a tint control before goint out of pins ① and ②. At pin ③ in generated a contrast control voltage.

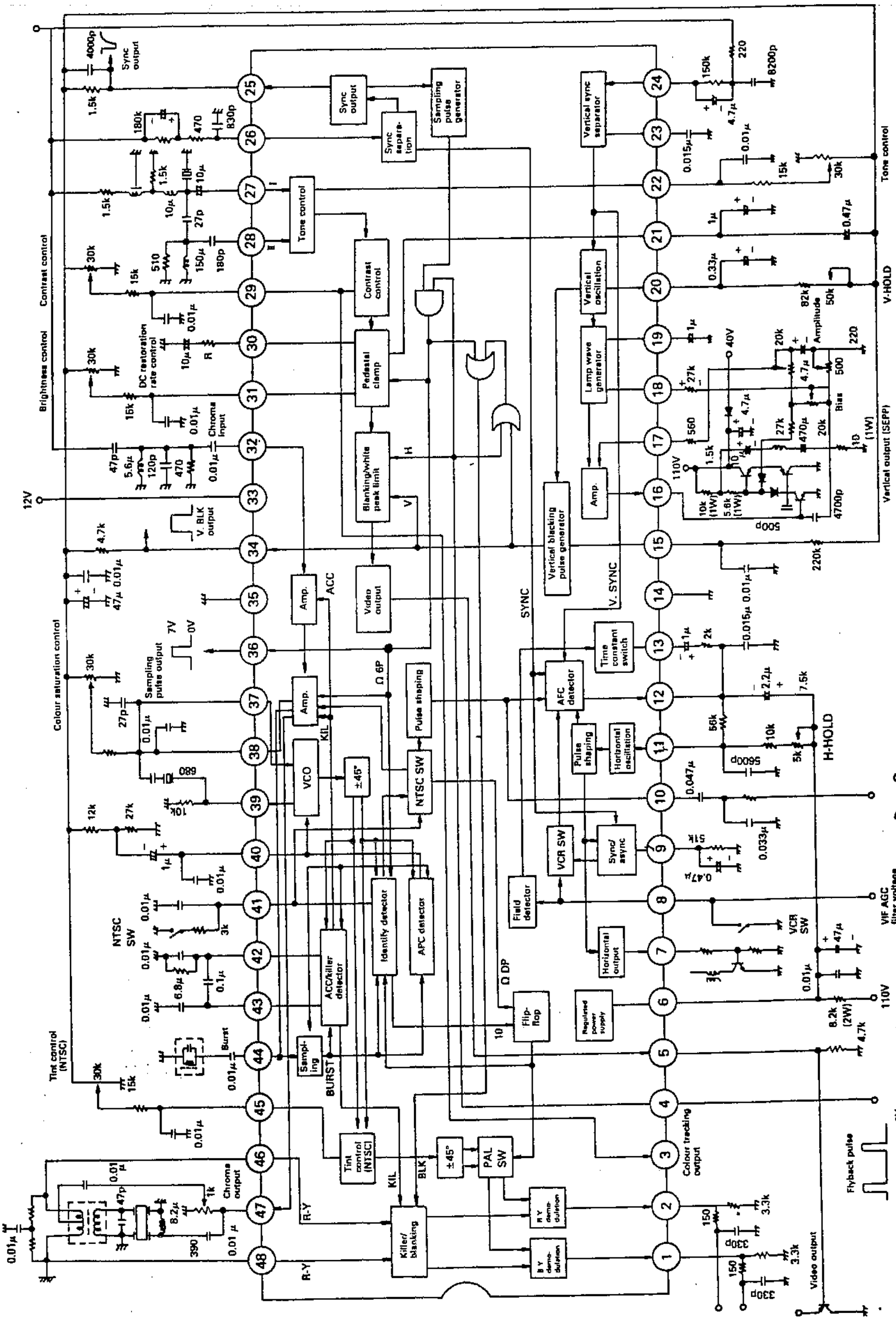


Figure 15. Block Diagram of IC801 (RH-IX0303CEN1)

5. SYNC SEPARATOR CIRCUIT

The sync separator circuit is provided with horizontal and vertical input pins and both pins are of the same emitter input system. The emitter input system tends to make lower the impedance of input signal resulting in a poor effect on processing of the incoming chroma signal and video signal. This, however, avoided by such design that the incoming IF signal is once applied to the buffer transistor and then delivered to input pins ㉖ and ㉔ of the sync separator circuit.
Pin ㉖ is for the horizontal sync separation and pin ㉔ for the vertical sync separation, and both separations are performed by almost the same circuit shown in Fig. 16.

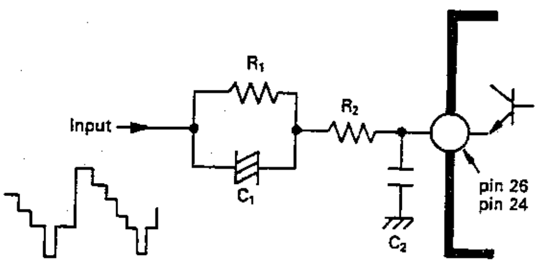


Figure 16.

The sync separation level is decided by the difference between the preset voltage at the input pin of IC801 and the sync tip DC voltage of incoming signal and also by the time constant of R_1, R_2, and C_1; C_2 is used for noise reduction at the time of weak field reception. And if the voltage at the input pin (㉖ or ㉔) is increased up to V_{CC} available at pin ㉝, it is allowed to forcibly stop the sync separation operation, which is convenient when servicing the TV set is needed.
Fig. 3 shows how the vertical sync separation output is processed. The separation output of pin ㉔ is inverted in phase and goes out of pin ㉓. Then it is subjected to a filter operation by the external capacitor and internal resistor (4.3 kohms) so that it trigger pulse to initiate the vertical oscillation. (See Fig. 17.)

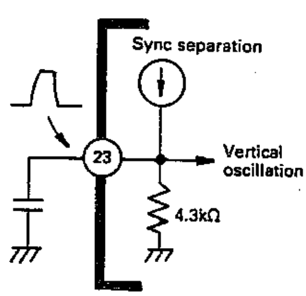


Figure 17.

Figure 18 shows how the horizontal sync separation output is processed. The separation output passes through emitter follower (PNP type) and goes out of pin ㉕: at the time, it is of a negative pulse which is made of DC 4V (sync tip voltage) and DC 12V (base voltage = V_{CC}).

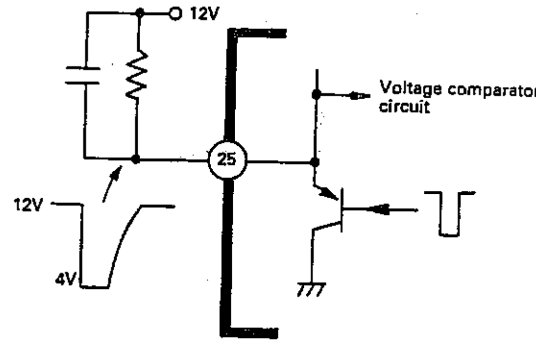


Figure 18.

It is here noted that there is generated BGP (Burst Gate Puse) at pin ㉕ in addition to the vertical sync separation signal. The CR delay circuit externally attached to pin ㉕ is used to slow down the rising edge of the vertical sync signal, and when the signal goes down to 9V, the end edge of BGP is detected. On the other hand, the front end of BGP is decided by the CR delay circuit located inside IC801, by which BGP timing is set at about 0.5 μsec in connection with the end edge of the vertical sync signal.
What is mentioned above is illustrated in Fig. 19.

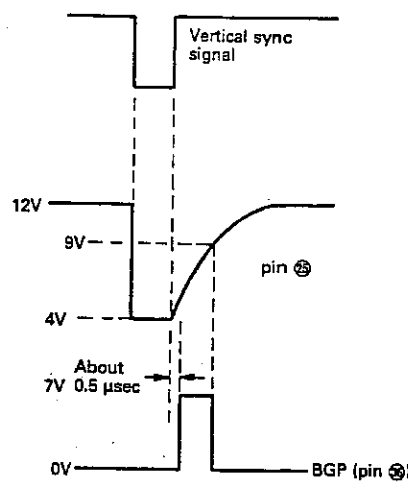


Figure 19.

The BGP thus produced is subjected to AND operation together with FBP (Flyback Pulse) coming from pin ④ and is supplied to the video/chroma circuit; then, it is also applied to the NPN emitter follower to have the ampliftude of 7 Vp-p and goes out of pin ㊱. The design of AND operation is intended to have the BGP be less affected by the noises which may be strongly caused at the time of weak field receiption, leading to an improved video/chroma characteristic at the weak field (see Step 8-3 described later).
There is a possibility that while the unit is in the video input mode, if no video signal is applied or the audio signal is mixed in the tuner by error, there is no chance where BGP is generated in the sync separator circuit. In this case, however, FBP may be used instead of BGP to allow the video/chroma circuit to start its operation. This is possible by decreacing the voltage at pin ㉕ to about 4V by means of resistor connected thereto.

6. HORIZONTAL DEFLECTION CIRCUIT

The horizontal deflection circuit consists of AFC circuit, sync detector circuit, horizontal oscillator circuit, horizontal output circuit and regulated voltage generator circuit.

6-1. Regulated voltage generator circuit

This circuit is of a series regulator system and generates a constant voltage of about 12V.

A reference voltage is resulted from the operation of two zener diodes (V_B = 5.3V) and two forward diodes (V_{BE} = 0.7V), and according to the reference voltage there is produced a constant voltage to be applied to the power supply pin ⑥ of the horizontal deflection circuit.

The current required to activate the whole unit of horizontal deflection circuit (with the regulated voltage generator circuit excluded) is of about 10 mA. This means that it is sufficient to keep the supply current at about 15 mA for a stabilized circuitry operation; however, to supply more current than this may provide an inconveniece in view of the current consumption.

6-2. AFC circuit

The AFC circuit is combined with the horizontal oscillator circuit (described later in step 6-3) and deflection output circuit (outside IC801) to form a PLL circuit.

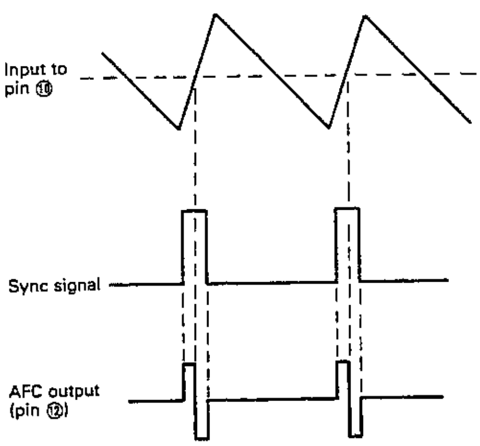


Figure 20.

Horizontal wave signal which has resulted from integration of FBP (Flyback Pulse) is applied to pin ⑩: at the same time, the sync signal coming from the sync separator circuit is supplied to the AFC circuit.

When the sync signal is at High level, there is a comparition between the actual voltage of the input signal at pin ⑩ and its means DC voltage. And if the former voltage is higher than the latter's, the current available at pin ⑫ goes out of there, and in the opposite case, an additional current from the external circuit flows thereinto. Then AFC output signal from pin ⑫ is sent to pin ⑪ of the horizontal oscillator circuit through a coupling resistor, where it is used for a PLL operation. In other words, if the input signal of pin ⑩ is delayed in phase, AFC output voltage becomes higher so that the oscillation signal of pin ⑪ will have an advanced phase; in the opposite case, the oscillation signal of pin ⑪ will have a delayed phase. There are rather significant ripples shown in Fig. 20, but in the actual circuit these are suppressed to the minimum by the included filter; and AFC detection sensitivity (μ) in the usual sync operation is set at about 180 μA/rad.

This AFC circuit is specially designed to provide a high performance even in the weak field and to meet the operation of VTR when connected to the TV set, the details of which will be discussed in Step 6-5 later.

6-3. Horizontal oscillator circuit and its output circuit

The horizontal oscillation circuit is composed of a time constant circuit (R_1 and C in connection with pin ⑪), Schmidt trigger circuit and R_2 (see Fig. 21-1).

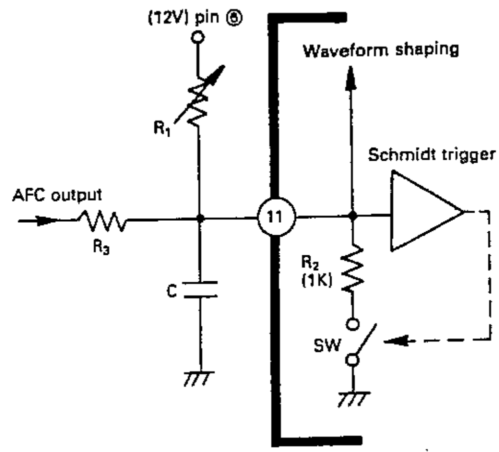


Figure 21-1.

The supply voltage for Schmidt trigger circuit is of 12V (at pin ⑥), and the threshold level of this circuit is set at 9V and 5V. When the supply voltage is higher than 9V, the threshold level goes down to 5V in which the switch (SW) is turned on; when it is lower than 5V, the threshold level goes up to 9V in which the switch is turned off. As a result, there is an oscillation signal at pin ⑪ whose waveform is as shown in Fig. 21-2: the rising edge of oscillation is decided by the time constant of R_1 and C while the falling edge by the time constant of R_2 and C; the free-run frequency is variable with change of the resistance of R_1.

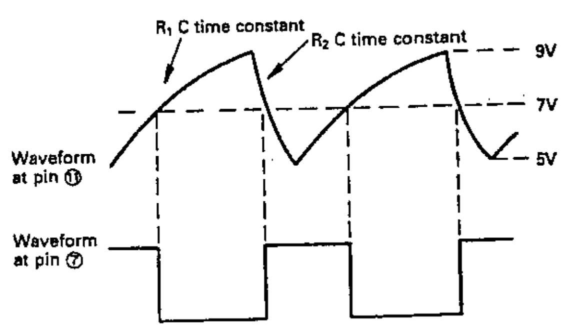


Figure 21-2.

Here is a PLL operation which is performed with use of the signal coming from pin ⑫ of the AFC circuit. The AFC signal is applied to pin ⑪ of this horizontal oscillator circuit through the coupling resistor R_3. When pin ⑫ is charged, the signal at pin ⑪ will have an advanced phase; when pin ⑫ is discharged, the signal will have a delayed phase. The oscillation control sensitivity (ß) is set at about 40 Hz/µA (R_1 = 12 KΩ, C = 5600 pF).
The oscillation waveform available at pin ⑪ is sliced by the voltage of 7V to produce a horizontal pulse (see Figs. 21-1 and 21-2), which goes out of pin ⑦. The output impedance of pin ⑦ is different depending upon whether the incoming signal is at High or at Low level; the difference is outlined in Fig. 22.

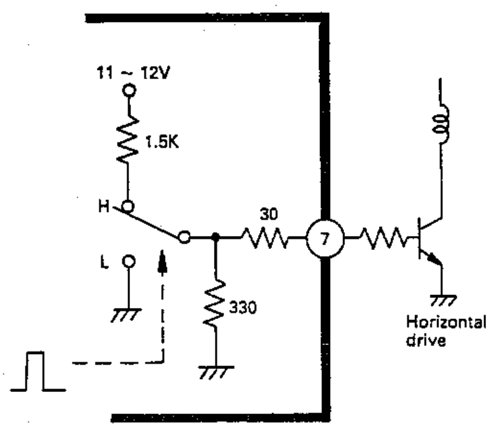


Figure 22.

6-4. Sync detector circuit

The output pulse of pin ⑦ of the horizontal oscillator circuit is applied to AND gate of the sync detector circuit while it is compared with the sync signal which is then available at that AND gate. As a result of AND operation, when both signals are found to occur in the same timing, the constunt current is allowed to flow in the circuit. Then the current is transformed into a voltage by the resistor and capacitor in connection with pin ⑨, and the voltage is used for various controls in the IC801 (see Fig. 23-1). It is here noted that the output pulse of pin ⑦ is used instead of FBP to be compared with the sync pulse for their sync detection. Therefore, should there occur an unusual operation to make abnormal the timing relation among the output pulse of pin ⑦, FBP and sync signal, the sync detector circuit fails to show a normal operation. The ideal relationship among the three signals is shown in Fig. 23-2, and this is always assured as far as the unit is operated in the normal manner in usual conditions.

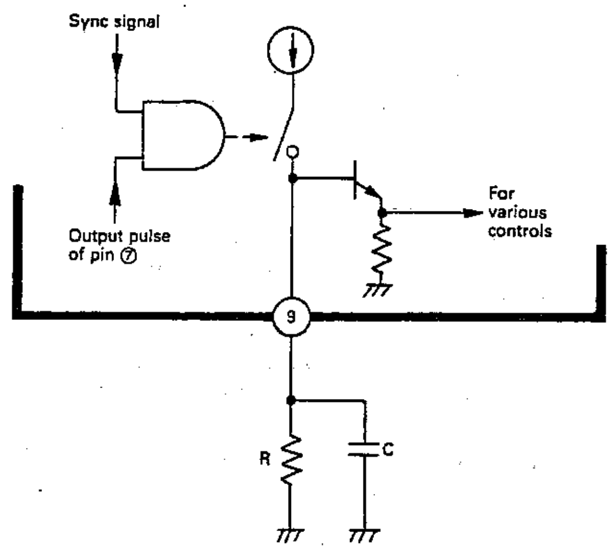


Figure 23-1.

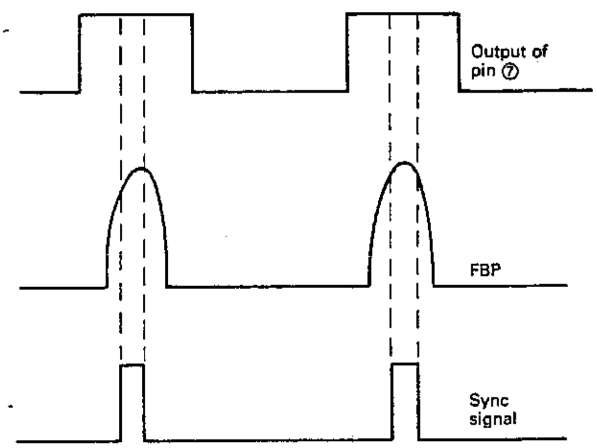


Figure 23-2.

6-5. Special behaviors of AFC circuit

The IC801 is provided with a special design that enables changeover of the time constant and loop gain of th AFC circuit, which aims at prevention of the horizontal jitters in the weak field as well as the skew distortion in the VTR's picture.

(1) Changeover of AFC loop gain
The AFC loop gain becomes High or Low level according to a variation of the AFC detection current available at pin ⑫. The loop gain is set at High level either when the VTR switch is turned on (with pin ⑧ forcibly grounded) or when the AFC circuit is in out-of-sync operation mode (with DC voltage of pin ⑨ being at lower than 1.2V). In other cases, the loop gain is set at Low level.

(2) Changeover of AFC time constant
Changeover of the time constant depends upon the fact the internal resistance of pin ⑬ is changed in continuous way by DC voltage coming from pin ⑧; Fig. 10 shows the relationship between the internal resistance of pin ⑬ and the DC voltage of pin ⑧. However, when the AFC loop gain is at High leve that is, when the VTR switch is turned on or the AFC

circuit is in out-of-sync operation mode, the resistance of pin ⑬ is set at maximum whatever voltage pin ⑧ may have.

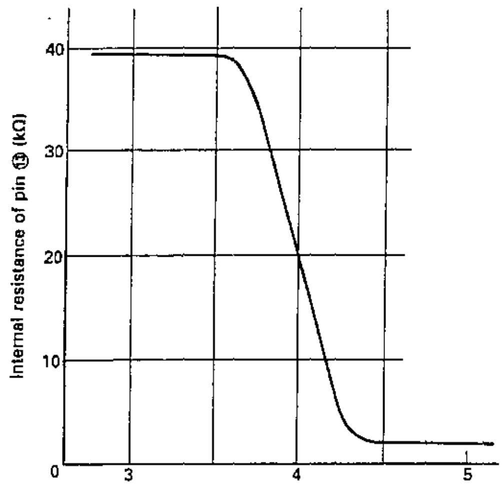


Figure 24.

(3) Behaviors of pin ⑧
DC voltage of pin ⑧ is varied according to whether the VTR switch is turned on or off, or to whether or not the unit is put in time constant control mode. When the VTR switch is turned on, DC voltage of pin ⑧ is set at less than 0.3V, where the AFC loop gain becomes High level and its time constant becomes minimum. When the unit is put in time constant control mode, DC voltage of pin ⑧ is variable in the range from 1.0V to 5.0V; and when it is lower than 3.5V, the time constant becomes minimum, and when it is more than 5.0V, time constant becomes maximum. In actual operation of the circuit, the DC voltage at pin ⑧ is controlled by the output of IF AGC circuit; that is, the output of pin ② of the IF AGC filter is supplied via the emitter follower circuit (NPN type) to pin ⑧.
The changeover of AFC time constant is allowed only when the unit is in in-sync operation mode (with DC voltage at pin ⑨ being more than 2.0V) provided that the loop gain is set at Low level. If pin ⑧ is made open, the time constant will be minimum.

(4) Behaviors of pin ⑨
The coincident filter connected to pin ⑨ is, as described in Step 6-4, used to judge whether the AFC circuit is in in-sync operation mode or in out-of-sync operation mode, and with its output voltage, changeover of the loop gain and time constant of AFC circuit is controlled. That is, when voltage is more than 1.8V, the loop gain is set at Low level while the time constant is changeable from minimum to maximum: when it is lower than 1.2V, the loop gain is set at High level while the time constant becomes minimum.
The voltage at pin ⑨ is variable depending on that the unit is in in-sync operation (strong and/or weak field), or in out-out-sync operation (with noise input only) or the unit is given no signal (and without any noise); and the variable range of this voltage is decided by the external resistor. And the larger the capacitance of the capacitor in parallel connection is, the faster the sync detection speed; and the smaller the capacitance is, the larger the vertical sag. With this taken in concideration, the AFC circuit is properly designed to provide its best performance. The voltage at pin ⑨ may also be used to cause audio muting as well as to activate the voltage synthesizer, but in this case, some means must be given not to impair a normal operation of the AFC circuit.

(5) Overall operation
What we have described before is summarized in Table 6 below from which it is seen how the loop gain and time constant of AFC circuit are controlled by DC voltages at pins ⑧ and ⑨.

Table 6.

Pin ⑧ / Pin ⑨	Over 0.3V (With VTR switch ON)	3.5V (Strong field) ~ 5V (Weak field)
Over 1.8V (In-sync mode)	• Loop gain: High • Time constant: Minimum	• Loop gain: Low • Time constant: Minimum ~ Maximum
Below 1.2V (Out-of-sync. mode)	• Loop gain: High • Time constant: Minimum	• Loop gain: High • Time constant: Minimum

The AFC circuit operates in this way to ensure better picture on TV and/or VTR screen. When the unit is at in-sync operation mode and with the VTR switch turned on, the loop gain of AFC circuit is at Low level and its time constant is changed from minimum to maximum, so that horizontal jitter in the weak field reception is limited to the least. And if the unit gets out of sync operation when the VTR switch is turned off, the loop gain is set at High level and the time constant becomes minimum, so as to widen the pull-in range of reproduced picture.
When the VTR switch is turned on, the loop gain is kept at High level with the time constant set at minimum so as to improve the skew distortion or reproduced picture.
The AFC circuitry operation is outlined in Fig. 25 below.
There is caused AFC output at pin ⑫, and this pin is connected to the voltage limiter (at the lower voltage side only) so that the oscillation frequency is prevented from going down exceeding the specified lower limit.

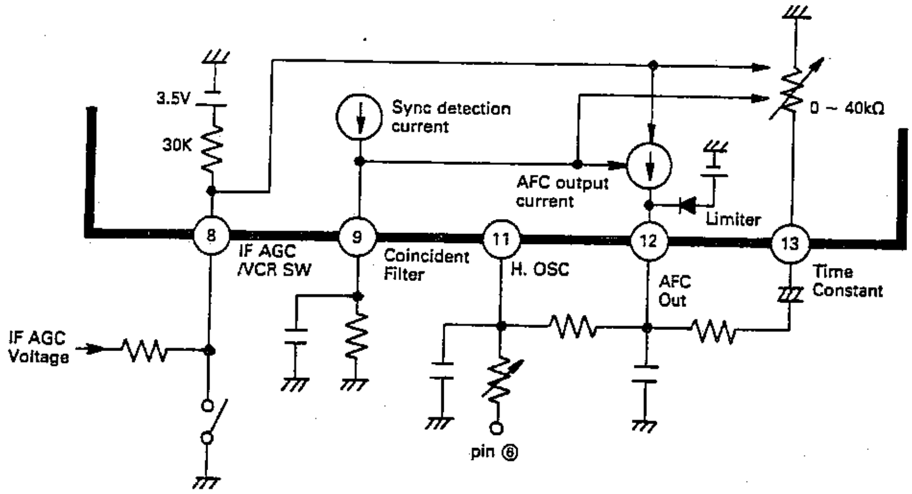


Figure 25.

7. VERTICAL DEFLECTION CIRCUIT

The vertical deflection circuit is composed of vertical oscillator circuit, lamp wave generator circuit, vertical output circuit and blanking pulse generator circuit.

7-1. Vertical oscillator circuit

The vertical oscillator circuit consists of a time constant circuit (R_1 and C in connection with ⑳), Schmidt trigger circuit as well as R_2 and switch SW (see Fig. 26-1).

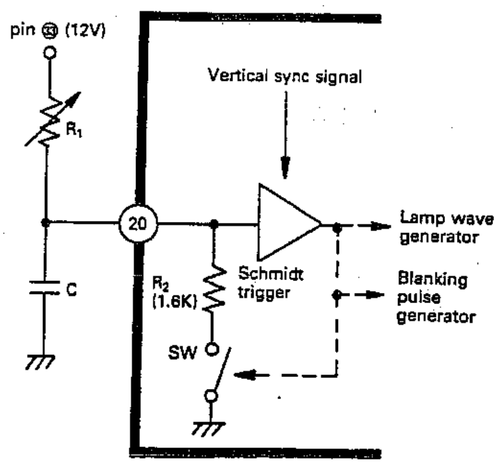


Figure 26-1.

The supply voltage for Schmidt trigger circuit is of 12V (at pin ㉝), and the threshold level is set at 8V (upper) and 4V (lower).

When the vertical sync signal is applied to Schmidt trigger circuit, the threshold level is decreased from 8V (the upper limit value) to 7.3V so that the vertical oscillation is triggered to produce a vertical oscillation pulse. The upper trigger-in level directly depends upon the vertical frequency while the lower one is decided by the factor of (vertical frequency × $\frac{7.3-4}{8-4}$): see Fig. 26-2.

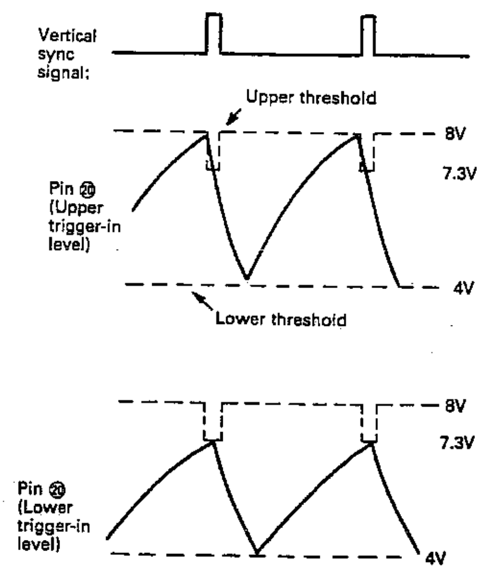


Figure 26-2.

This IC is designed to operate with a rather low current consumption, and this makes the horizontal frequency fluctuation liable to affect the power source, leading to a mal-effect to the interlace operation. To avoid this, due care must be taken for parts allocation and leads arranement on the PWB.

7-2. Lamp wave generator circuit

The constant voltage circuit in the lamp wave generator circuit is turned on when the vertical oscillation is at its rising edge (with the switch SW turned on: see Fig. 26-1), so that the capacitor in connection with pin ⑲ is instantly charge up. And a current then available at pin ⑲ is applied to pin ⑱; the amperage of this current is decided by the resistor connected to pin ⑱. So that the lamp waveform signal as shown in Fig. 27-2 is generated and sent to the vertical output circuit.
The voltage from the constant voltage circuit is kept at about 6.6V. The constant current which runs in pin ⑱ is decided by resistance division of the power supply voltage; the former varies in proportion to the latter.

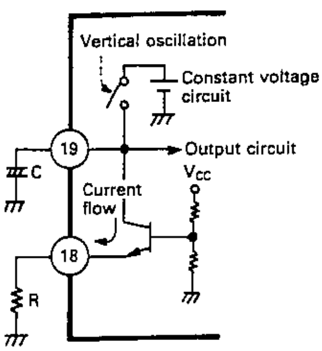


Figure 27-1.

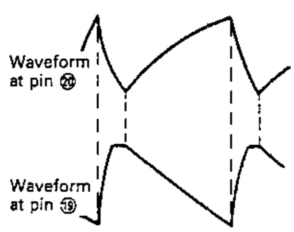


Figure 27-2.

7-3. Vertical output circuit

Fig. 28 shows the vertical output circuit. The lamp waveform signal is amplified in the amplifier (about 45 dB), the output of which is sent to pin ⑯. This signal output is enabled with the current consumption as low as about 15 mA, to meet the operation of SRPP circuit. AC and DC components of the output signal are made together to be fed back to pin ⑰.

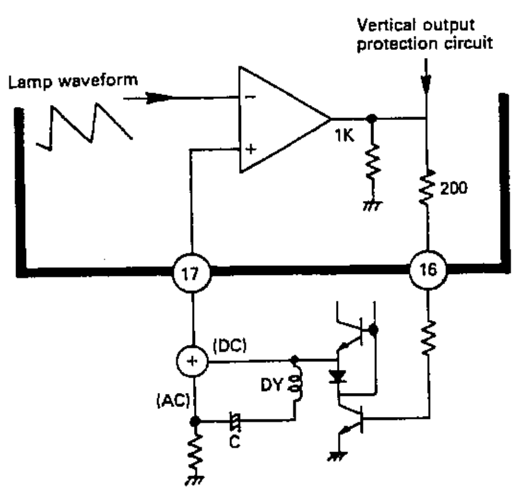


Figure 28.

If the power supply voltage (at pin ㉝) of the IC goes up too high due to something abnormal, the vertical protection circuit works to prevent the voltage at pin ⑯ from lowering down excessibly, so that the output capacitor ("C" in Fig. 28) is protected against damages by the higher voltage.
If it is needed at the time of servicing to stop the vertical oscillation forcibly, this can be done by applying a high voltage to pin ⑯ or ⑰ forcibly, or a low voltage to pin ⑳ (at the oscillator circuit) and pin ⑲ (at the lamp wave generator circuit) also forcibly. However, it is here noted that if the voltage at pin ⑳ is lowered down to below 1.5V, the transistors inside the IC may be damaged, and that if pin ⑲ is given a lower voltage, this will cause the current of a few 10 mA at least to flow in pin ⑲ from V_{CC}.

7-4. Vertical blanking pulse generator circuit

Fig. 29-1. shows the vertical blanking pulse generator circuit. When the vertical oscillator circuit starts to discharge itself, the switch SW in the vertical blanking pulse generator circuit is opened to charge pin ⑮ through the capacitor and resistor externaly connected to this pin, thus to initiate the blanking operation. As charging at pin ⑮ proceeds and its voltage reaches about 5V, the switch SW is closed to terminate the blanking operation. The blanking operation starts in timing with the rising edge of the vertical sync output and how long it lasts is decided by the time constant of the capacitor and resistor in connection with pin ⑮.
The blanking pulse thus produced is then applied to the video/chroma circuit for blanking of the video and chroma signals, and at the same time goes out of pin ㉞ through the open collector circuit.
The output available at pin ㉞ is at High level at the time of blanking with the maximum rating of 3mA and 16V.
Fig. 29-2 shows the timing relation among the waveforms accompanying the vertical oscillation.

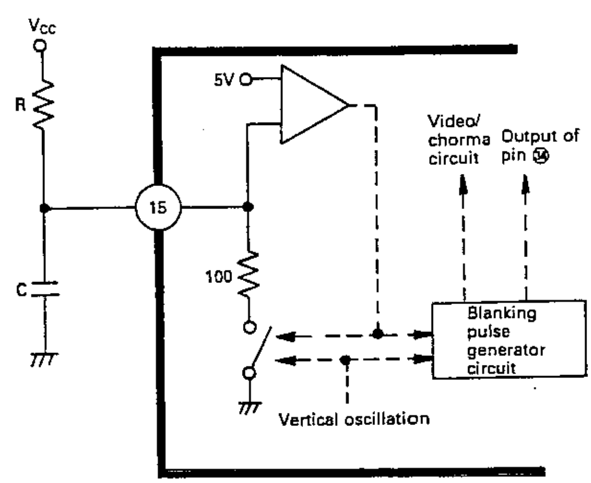


Figure 29-1.

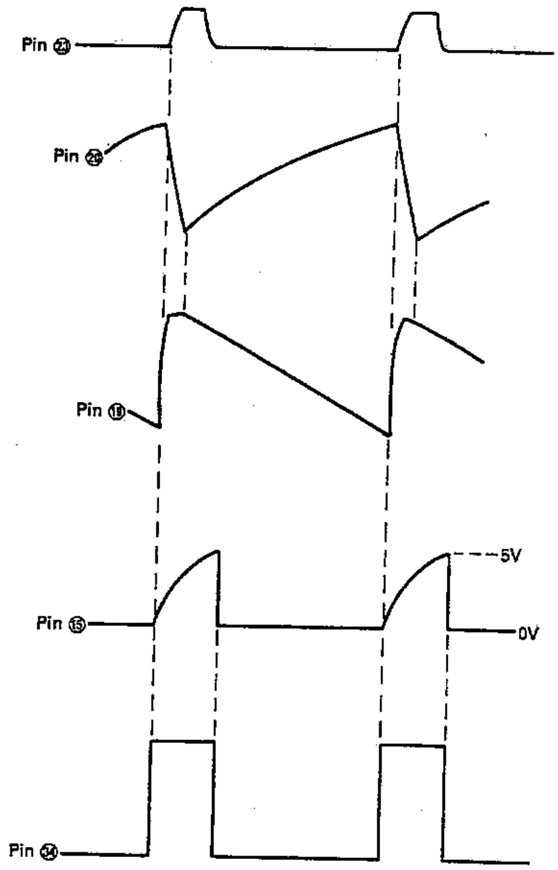


Figure 29-2.

The resistor which is externally connected to pin ⑮ is usually designed to have its resistance greatly more than that of the internal resistor (100 ohms): it is desirable for the external resistance to be more than 100 kohms. Without this design, the discharge voltage of pin ⑮ fluctuates because of IC quality dispersion or the environmental temperature, resulting in an instability of the blanking length of time.

8. VIDEO CIRCUIT

The video circuit is composed of video amplifiers (tone/contrast control), DC restoration circuit (brightness control) and output circuit (white peak limiter, horizontal/vertical blanking).

8-1. Video amplifiers

As shown in Fig. 30-1, there are three amplifiers for tone control and one amplifier for contrast control which are included in the video circuit.

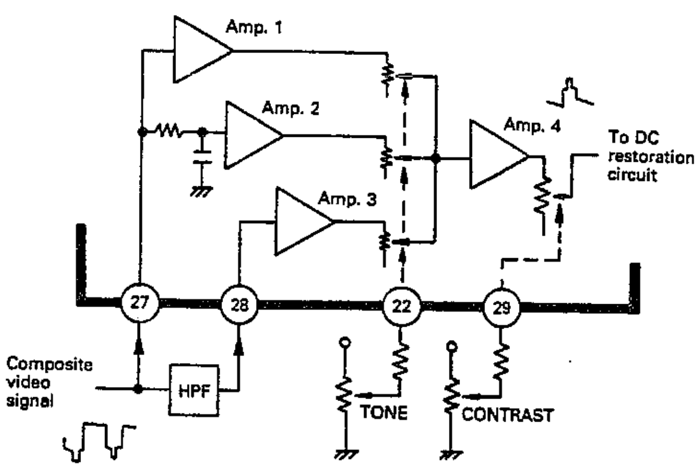


Figure 30-1.

The composite video signal which has passed through the delay line and colour signal trap is applied to pin ㉗ and, at the same time, is sent to pin ㉘ via the high pass filter.

The video signal going out pin ㉗ is then fed to the amplifier 1 and, at the same time, is sent to the amplifier 2 via the low pass filter. The high-frequency component of the video signal available at pin ㉘ is applied to the amplifier 3. Then each of the three amplifiers is subjected to gain control by DC voltage available at pin ㉒: Figs. 30-2, -3 and -4 show how the amplifiers are varied respectively in their gain. The respective outputs of the three amplifiers are added together in such way as to obtain the ideal tone of reproduced picture: Fig. 31 represents a typical example of the tone control characteristic thus obtained. The video signal, after having experienced the tone control, is then supplied to the amplifier 4 where it is subjected to the contrast control Fig. 32 shows a typical example of the contrast control characteristic achieved there.

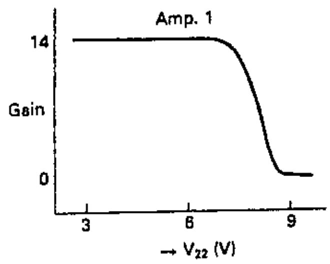


Figure 30-2.

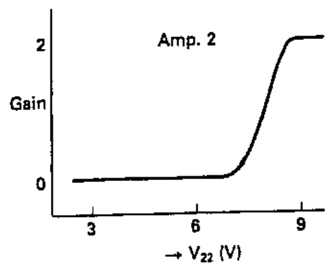


Figure 30-3.

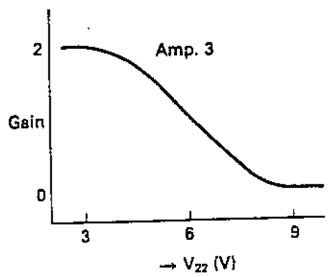


Figure 30-4.

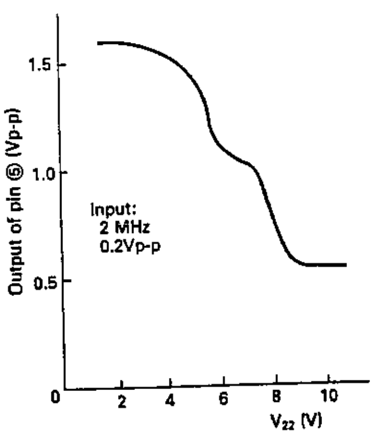


Figure 31.

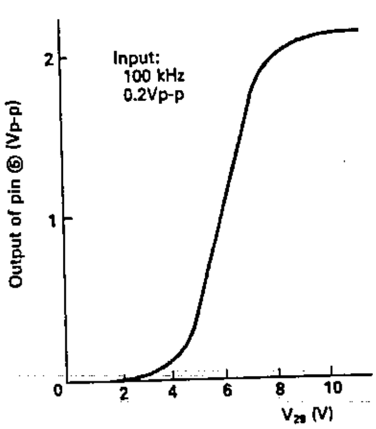


Figure 32.

8-2. DC restoration circuit

Fig. 33-1 shows an outline of the DC restoration/ brightness control circuit.

The video signal which has experienced the tone/ contrast control is here amplified by the rate of R2/R2 in the circuit of Q_1, R_1, Q_2 and R_2, and at the same time its DC level is controlled by the voltage at the base of Q_2.

This DC level control is performed in the way that: there is a DC difference voltage between pins ㉛ and ㉚, and the difference voltage is amplified to be applied to the base of Q_2 only during BGP (Burst Gate Pulse) period so that C_1 and C_2 in connection with pin ㉑ is charged up. Accordingly, the voltage at the base of Q_2 remains the same even when it is out of BGP period.

During BGP periode, it is seen from Fig. 33-1 that DC voltage at pin ㉛ is inversed in phase and fed back to pin ㉚. In this way, it is possible during BGP period to control DC voltage (pedestal DC voltage) at the emitter of Q_3 by applying a brightness control voltage to pin ㉛. Fig. 33-2 represents the brightness control characteristic.

If C_3 in connection with pin ㉚ is grounded, the video signal appearing at the emitter of Q_3 is integrated by R_3, R_4 and C_3 to get under the brightness control; at this time, DC voltage of the video signal is controlled at the DC restoration rate of $R_4/R_3 + R_4$. With pin ㉚ kept opened, the DC restoration rate is set at 100%. C_1 and C_2 in connection with pin ㉑ are used to improve the transient response characteristic (just when the power switch is turned on).

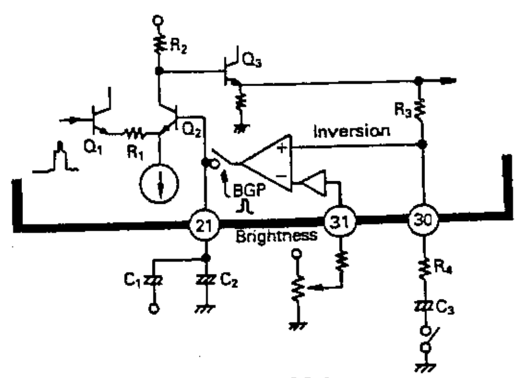


Figure 33-1.

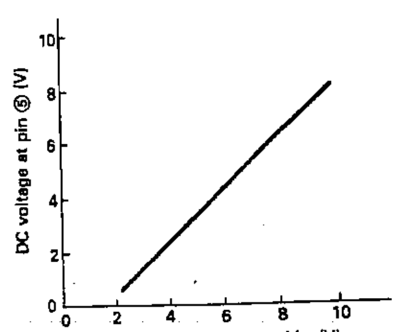


Figure 33-2.

8-3. Output circuit

The signal going out of the DC restoration circuit passes through the 2-stage transistor (Q_1 and Q_2 shown in Fig. 34) is applied to pin ⑤. At the base of Q_1, DC voltage of the signal has the temperature characteristic of 0 V_{DE} and when it reaches pin ⑤, it will have the temperature characteristic of 2 V_{BE}.

The output signal of pin ⑤ is subjected to its DC voltage control by Q_3, Q_4 and Q_5 : Q_3 is effective during the vertical blanking period; Q_4 during the horizontal blanking period; Q_5 during WPL (White Peak Limiter) operation.

At the time of vertical blanking, the voltage at the base of Q_3 becomes higher, to which the output voltage of pin ⑤ is clamped. At the time of horizontal blanking, the FBP (flyback pulse) is applied to pin ④ while the output voltage of the comparator circuit becomes higher (if given more than 9V), to which the output voltage of pin ⑤ is clamped by means of Q_4. The WPL operation is performed in the way that: if pin ④ is given some DC voltage when it is out of FBP period, the output voltage of pin ⑤ lowers down to the voltage at the base of Q_5 minus V_{BE}.

The output signal of the comparator circuit is sent to the BGP generator circuit and AND circuit where a burst gate pulse is produced for various controls in the IC801.

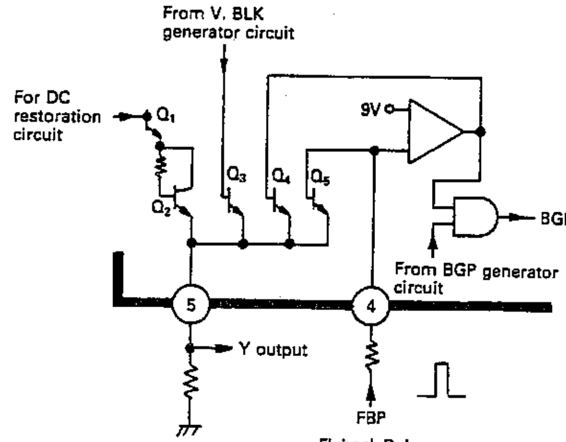


Figure 34.

9. CHROMA CIRCUIT BLOCK

The chroma circuit is composed of the following blocks; the main signal processing section consisting of chroma amplifier and colour output demodulator circuit, and the section for the burst signal processing and main signal control which is composed of ACC/killer detector circuit, identify detector circuit, APC detector circuit and VCO circuit. For convenience of the explanation, the descriptions will be given first on how the burst signal is processed and how the main signal is controlled. Though this IC is designed to have priority for PAL system, it can also receive signals of NTSC system. The explanations will be given for both systems where their operations are different.

9-1. VCO circuit/APC circuit

The VCO (Voltage Controlled Oscillator) circuit and APC (Automatic Phase Control) circuit work to carry out a PLL operation, so that a CW (Carrier Wave) signal is generated to be locked with the burst signal. The carrier wave is then used to activate the ACC/killer detector circuit, identify detector circuit and colour output demodulator circuit.

As shown in Fig. 35, the VCO circuit is composed of the amplifier and phase composition circuit, both located between pin ㊲ and pin ㊴, and the externally connected crystal loop. The external crystal loop is made of series resonation LC, and its oscillation frequency is variable with change of the phase of IC by means of the APC filter voltage. More precisely, the oscillation wave available at pin ㊲ is amplified and divided into two signals which have different phases. The composition of these signals is controlled by the APC filter voltage coming from pin ㊵, thus altering the phase of the output signal of pin ㊴; as the voltage of pin ㊵ is increased, the output signal of pin ㊴ is lagged in phase with its free-run frequency decreased. R_1 is a load resistor to meet the output of pin ㊴ which is connected to the open-emitter transistor; R2 is a damping resistor for the resonation circuit; and C_1 is a trimmer capacitor to adjust a deviation of the free-run frequency due to a quality dispersion of the IC and its peripheral circuits. The larger deviation of free-run frequency will result in that the pull-in range of VCO is biased to make shallower the killer level and that the identify detector circuit is liable to cause erroneous locking with the burst signal. C_2 is a low pass filter which works to prevent abnormal oscillation due to overtoning of the external crystal loop: if the capacitance of C_2 if too high, the contro. range of VCO becomes narrower with its pull-in range and holding range also becoming narrower.

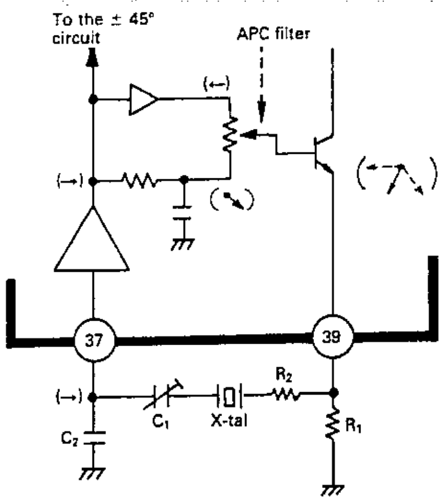


Figure 35.

The output signal of the VCO circuit is sent to the ± 45° circuit where it is divided into +45° CW (carrier wave) signal and −45° CW signal. The −45° CW signal is then supplied to the APC detector circuit the outline of which is shown in Fig. 36-1. The −45° CW signal is here multiplied with the burst signal, and the resultant signal is subjected to a sampling operation during BGP period and to a holding operation during non-BGP period. Fig. 36-2 shows the phase relationship between the −45° CW signal and burst signal when they are normally locked with each other.

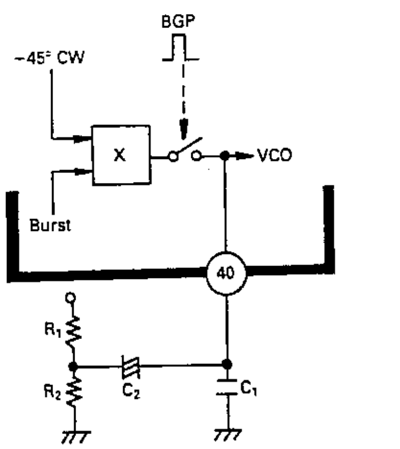


Figure 36-1.

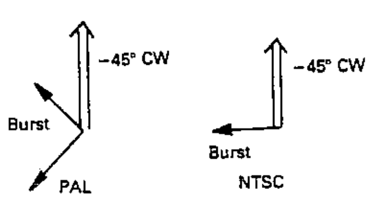


Figure 36-2.

When the phase of the −45° CW signal is lagged, DC voltage of pin ⑩ decreases and its output frequency becomes high with lagged phase. When the phase of the −45° CW signal takes a lead, on the contrary, DC voltage of pin ⑩ increases and its output frequency becomes low with lead phase. In this way, the CW signal is locked with the burst signal.

As is well known about the PLL circuit, if the time constant (provided by C_2, R_1 and R_2 in this case) of the included low pass filter is small, the anti-noise characteristic will deteriorate; and if it is large, the pull-in range of VCO becomes narrower.

The R_1/R_2 ratio exerts an influence on the transient response characteristic when the power switch is turned on. The representative value of APC detection sensitivity (μ) is 35 mV/deg. and that of the VCO control sensitivity (ß) is 2.8 Hz/mV. The principles of VCO pulling-in operation are shown in Fig. 37.

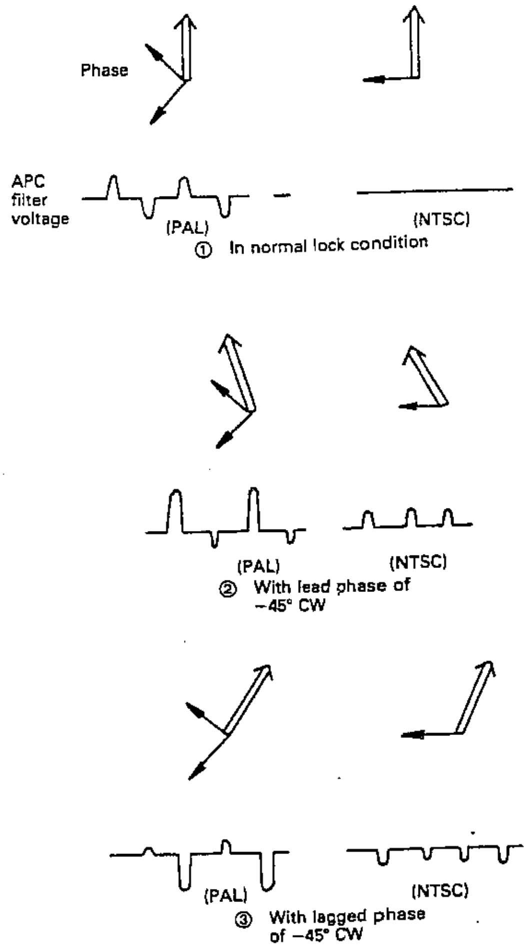


Figure 37.

9-2. Control of CW phase (±45° circuit and tint control circuit)

Fig. 38 shows the phase relation of each CW against the burst signal when they are normally locked with each other.

The tint circuit controls the degree of composition of ±45° CW and changes the CW phase in the demodulator circuit to control the demodulation angle.

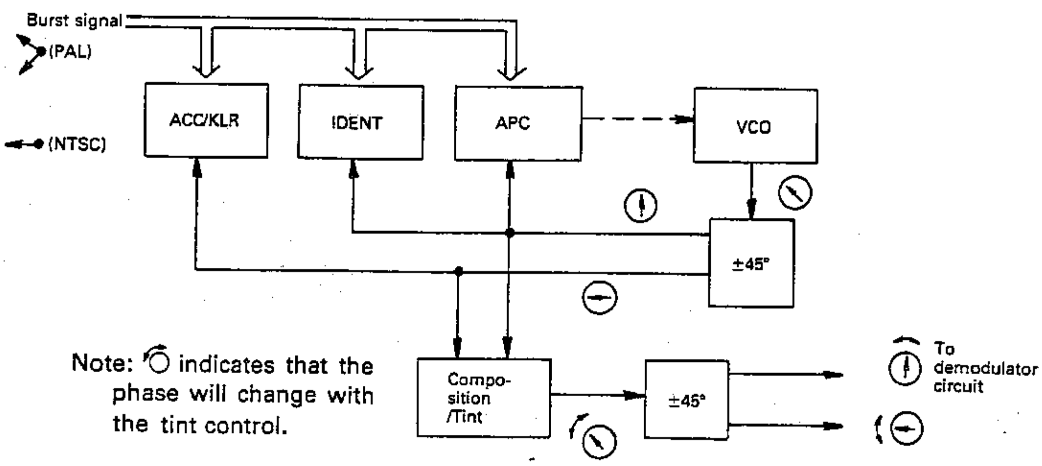


Figure 38.

9-3. Identify detector circuit, NTSC switch circuit and flip-flop circuit

R-Y component of PAL signal has its phase reversed alternately every 1H, and to meet this operation, the burst signal also changes its phase from +135° to −135° and vice versa every 1H. The identify detector circuit works to detect in what timing the burst signal's phase is changed from +135° to −135° and vice verse every 1H. The flip-flop circuit is used to reverse the phase of each control signal every 1H.

The horizontal sawtooth signal available at pin ⑩ is applied to the comparator circuit where it is shaped in waveform to become a control pulse to drive the flip-flop circuit. The reference voltage of the comparator circuit is set at 250 mV lower than the average DC voltage of the horizontal sawtooth signal. To have a stablized operation of the flip-flop circuit, it is desirable to keep the amplitude of pin ⑩ at more than 1 Vp-p. Fig. 39 illustrates the principle of what we have mentioned above.

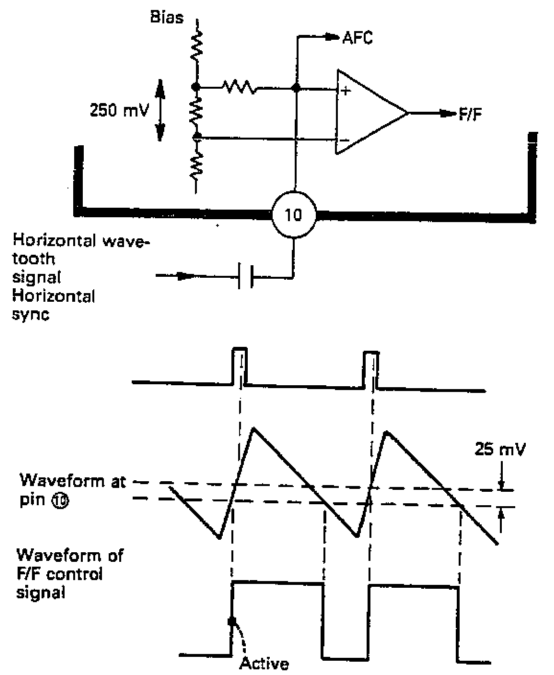


Figure 39.

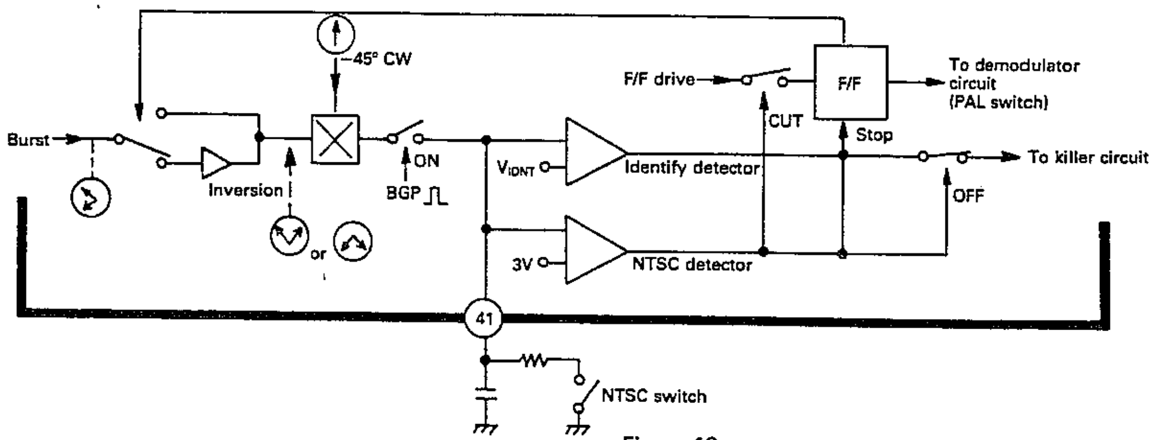


Figure 40.

Fig. 40 shows the outline of the identify circuit and NTSC circuit.
The output signal of the flip-flop circuit is reversed in phase every 1H so that the burst signal's phase is also reversed every 1H. The burst signal is then multified by −45° CW and the resultant signal is subjected to a sample/hold operation by the capacitor in connection with pin 41. The voltage as a result of the sample/hold operation is compared with the reference voltage which is slightly lower than DC voltage (V_{IDENT}) equivalent to the multiplied output under no signal condition. In case of erroneous circuitry operations, the voltage of pin 41 becomes lower than the value of V_{IDENT} and the flip-flop circuit is temporarily put in a stop while the chroma amplifier experiences a killer operation. Fig. 41 shows the principle of these operations.

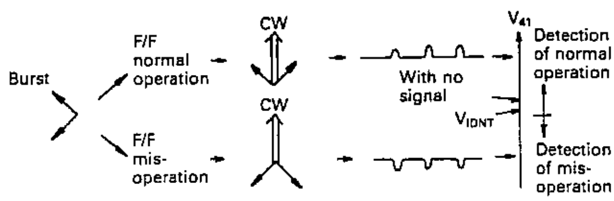


Figure 41.

The operation speed of the identify circuit is increased by making smaller the capacitance of the capacitor which is connected with pin 41; the killer operation which accompanies a mis-operation of the identify circuit is performed also at high speed, because it takes place in the later stage than the colour control operation, which is different from the ordinary killer operation described later.
No identify operation is needed when the unit is receiving NTSC signal, and so there are two different voltages at pin 41 to meet either the identify operation during PAL system mode or the non-identify operation during NTSC system mode. Namely, the voltage of pin 41 is kept at 8V to 9V to allow indentify operation for PAL mode, while it is forcibly reduced to lower than 3V (with the resistor of 3kΩ grounded) to meet nonidentify operation at NTSC mode. When the voltage of pin 41 is reduced to lower then 3V, another comparator detects that the unit is operating in NTSC mode, so that generation of the pulse to drive the flip-flop circuit is stopped and the killer operation which accompanies a mis-operation of the identify circuit is also put off forcibly. In this way, the flip-flop circuit stops its operation in NTSC mode, in such direction as to allow normal operation of the next-stage demodulator circuit.

9-4. ACC/chroma killer detection circuit

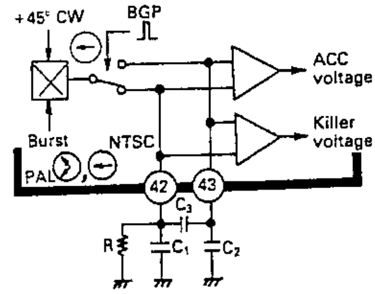


Figure 42-1.

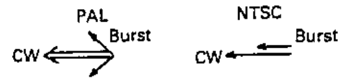


Figure 42-2.

Fig. 42-1 shows the outline of the ACC (Automatic Chroma Control)/chroma killer detection circuit. The burst signal and +45° CW are multiplied by each other having the respective phases shown in Fig. 42-2, and the resultant signal is used to charge either pin 42 during BGP period or pin 43 during non-BGP period; the potential difference between pins 42 and 43 varies according to the amplitude of the incoming burst signal. When the amplitude is large, DC voltage of pin 42 becomes high.
The voltage available at pin 43 is the multiplied output without burst signal, which accurately follows the output fluctuations of pin 42 due to the deviations of power supply, temperatures, etc. (this behavior is usually called as a bias sampling hold operation). Accordingly, the exact multiplied output can be obtained as a potential difference between pins 42 and 43.
This IC performs the burst level detection based on the sync detection system, and in addition to this, the burst level is decided by the above-mentioned bias sampling hold operation so that the deep and stabilized killer level is realized. The killer level is decided by the design that the resistor R in connection with pin 42 is used to provide an offsetting between pins 42 and 43. The ACC level also depends on this resistor R although it has been almost set by the IC itself.
C_3 is used to determine the transient response characteristic (when the power switch is turned on and off, or the killer circuit is turned and off), the ACC operational performance (vertical sag) during the vertical sync period, and the anti-noise characteristic in the weak field reception: the time constant of C_3 is set to the optimum to obtain the purpose, together with optimum selection of the time constant of the APC filter (connected with pin 40). C_1 and C_2 are used not only to charge or discharge pins 42 and 43 but also to perform the role of filtering the high frequency component out of the multiplied output; to attain the purpose, the ceramic capacitors (0.01 μF) with good high frequency characteristic are employed. The same consideration is given to designing of the APC filter (connected with pin 40) and the identify filter (connected with pin 41).

9-5. Burst cleaning/sampling

The burst signal coming from the chroma amplifier circuit described later is applied to pin ㊹ through the impedance of about 2.5 kohms, and at the same time, it is sent to the burst signal sampling circuit during BGP period where only a pure burst signal is picked out. Then the burst signal is fed to each of the APC detector circuit, ACC/killer detector circuit and identify detector circuit where it is multiflied by the CW signal available with each of these circuits.

To pin ㊹ is connected the external capacitor and tank circuit which are used to perform the cleaning of burst signal (see Fig. 43). C_1 is the capacitor to cut off DC voltage of pin ㊹, and L and C_2 are the tank circuit.

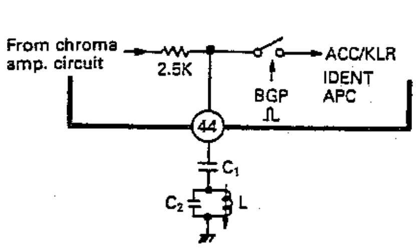


Figure 43.

The tuning point of the tank circuit can be checked by monitoring the chroma output of pin ㊾ which is available when the burst signal present at pin ㊹ is kept under the control of ACC detector circuit. And when the tank circuit is set at its best turning point, the burst signal of pin ㊹ is maximum as it enters the ACC/killer detector circuit, so that there is produced the minimum chroma output at pin ㊼.

If the tuning point of the tank circuit is changed, the phase of the burst signal which is applied to the APC detector circuit is also changed. This means that it is possible to adjust the phase difference between the demodulated chroma signal and CW signal by changing that tuning point.

To keep higher the value Q of the tank circuit is better because making it too low will diminish the cleaning effect and deteriorate the weak field characteristic. If the value Q is made too high, however, the cleaning effect is reduced since it also depends on the internal resistor of 2.5 kohms.

Problem on the free-run frequency, one of the commonly discussed problems about the chroma circuit, is caused mostly due to roundabout or interference resulting from the arrangement of parts or leads on the IC. To keep the circuit in Fig. 44-1 free from this problem, it is required to arrange the parts and leads on the IC so as to make the least the turnout of CW at pin ㊹ when it is given no chroma signal.

9-6. Chroma amplifier

The main signal is processed in the chroma amplifier and also in the demodulator circuit described later. Fig. 44-1 is a block diagram of the chroma amplifier. The signal passing through the band pass filter, where only the chroma component is taken out, is supplied to pin ㉜ and amplified in the primary ACC amplifier (A).

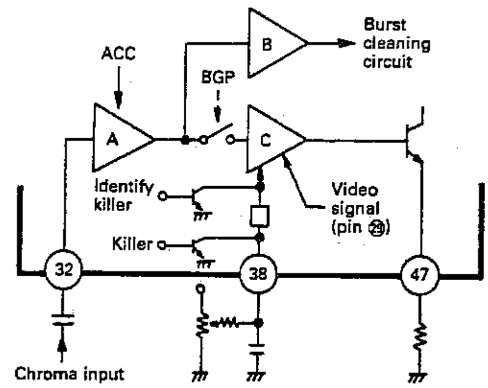


Figure 44-1.

The gain of the ACC amplifier is about 20 dB at maximum, and it is controlled by the output signal of the ACC/killer detection circuit so that the chroma signal output of the amplifier is kept always constant. Fig. 44-2 shows an example of the ACC characteristics.

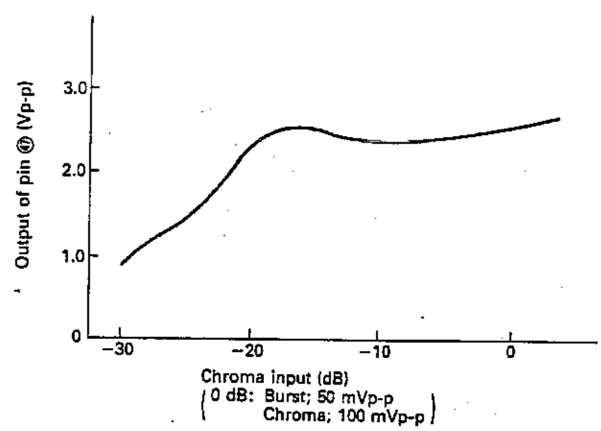


Figure 44-2.

The chroma signal going out of the ACC amplifier is then sent to the burst amplifier (B) or the colour control amplifier (C) in the next stage. The amplifier (B) and the amplifier (C) are shown independently in Fig. 44-1, but in actual cases most of their parts are co-used according to the design which makes the maximum gain of the amplifier (C) completely equal to the fixed gain of the amplifier (B).
In the amplifier (B), the chroma signal is amplified by about 27 dB and sent to the burst cleaning circuit. The chroma signal then available at the burst cleaning terminal (pin ㊹) includes not only the burst component but also the main signal component, and it is in the later stage that only the burst signal will be taken out of the chroma signal. In the amplifier (C), on the other hand, there is no signal input during BGP period so that there appears no burst signal at pin ㊼; this behavior is specified to make the 1H delay line connected with pin ㊼ free from the interference by the burst signal.
The gain of the amplifier (C) is variable with change of DC voltage at the colour saturation control terminal (pin ㊳). With regard to the colour saturation for which the final colour tracking is done by the SECAM chroma IC, it is arranged that DC voltage of pin ㉙ is directly applied to the buffer and goes out of pin ③ entering the SECAM chroma IC. Therefore, the gain of the amplifier (C) is fixed with the maximum contrast and is variable with change of DC voltage of pin ㊳. Fig. 44-3 shows the colour saturation charactristic.

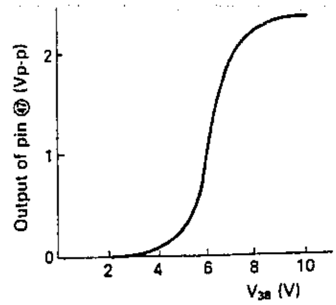


Figure 44-3.

The killer operation is performed in the following order. The normal killer detection output is applied to pin ㊳, and DC voltage then available at pin ㊳ is reduced to the level almost close to the ground voltage. By doing so, the gain of the amplifier (C) is lowered so that the chroma signal is disabled to go out of pin ㊼. In practice, whether the killer operation is working or not can be confirmed by measuring DC voltage at pin ㊳.
As to the killer operation which accompanies a mis-operation of the identify circuit, it is activated in the circuit which is provided after the buffer circuit away from pin ㊳. Thus the operation is performed at high speed regardless of the time constant of the resistor which is connected with pin ㊳. The signal output of pin ㊼ is allowed through the open emitter transistor and it is designed that it can be driven up to about 6 mA (with the emitter resistance of 1 kohms) in view of coopera-tion with the 1H delay line in connection with pin ㊼.

9-7. Demodulator circuit

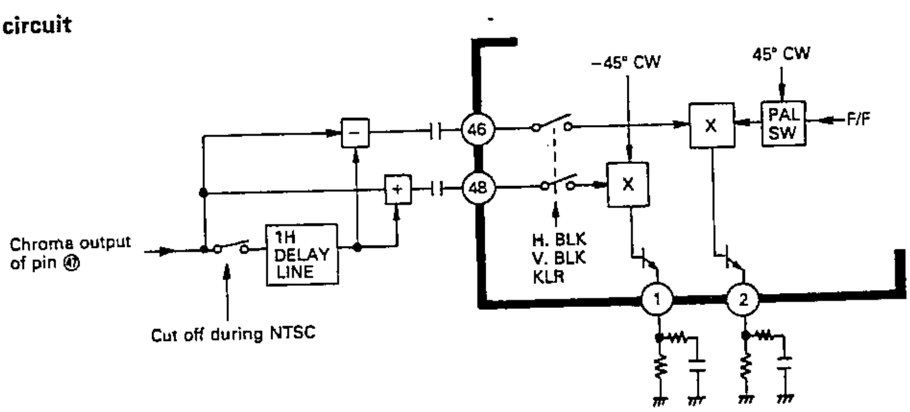


Figure 45-1.

Fig. 45-1 shows the outline of the demodulator circuit. The chroma signal coming from pin ㊼ is partially applied to the 1H delay line, and the signal thus delayed and the not-delayed signal are subjected to addition or subtraction to produce B-Y signal and R-Y signal, which are then sent to pins ㊽ and ㊻ respectively: in the case of NTSC system, only the not-delayed signal is supplied to pins ㊽ and ㊻ simultaneously. After that, B-Y signal and R-Y signal are sent to their multiplier circuits for their demodulation; here is noted that no input is applied to the multiplier circuit during the horizontal and/or vertical blanking period or when the killer circuit is in operation. B-Y signal available at pin ㊽ is multi-plied by −45° CW signal, and the resultant signal goes out of pin ①; this output refers to B-Y demodulation output. R-Y signal available at pin ㊻ is multiplied by +45° CW signal the phase of which is reversed every 1H by the flop-flop output controlled in normal direction with the identify circuit, then the resultant signal goes out of pin ②; this output refers to R-Y demodulation output.

The ratio of each demodulation output is set as per standard according to the resistance ratio of the IC itself, and its fluctuations are limited to the least against possible deviations of power supply, temperature, etc. Take note, however, that the demodulation ratio is set with a priority given on PAL system and in case of NTSC system the ratio slightly differs from the standard value. Fig. 45-2 shows the demodulation characteristic.

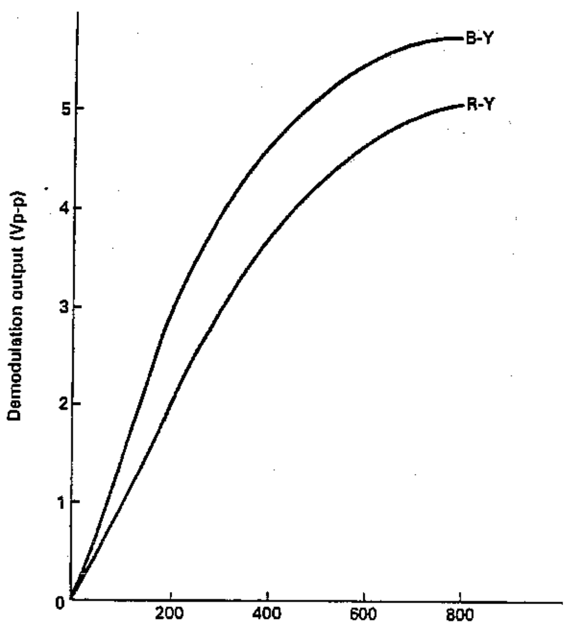


Figure 45-2.

When the unit is in NTSC reception mode, the output voltage of pin ㊺ of the tint control circuit is used to change the phase of CW signal to perform the tint control during NTSC reception. However, the demodulation angle between B-Y signal and R-Y signal is fixed at 90° for NTSC system, and this means that the demodulation angle of NTSC standard won't be precisely set even with the said tint control.

This tint control circuit also works while the unit is in PAL reception mode: in this case, pin ㊺ is kept opened to obtain the normal demodulation angle. The reason why the demodulator circuit needs a killer operation is as follows. In case the SECAM chroma IC is included in the unit, the same 1H delay line is used for both SECAM reception and PAL reception. When the unit is in SECAM reception mode, the SECAM signal is applied to pins ㊻ and ㊽, then it passes through the demodulator circuit and goes out of pins ① and ②. After that, the signal is sent to the SECAM chroma IC where it is judged whether it belongs to SECAM system or to PAL system. During this process, however, there is much traffic of the signal between each IC to cause such inconvenience as cross-talk. To avoid this crosstalk, it is designed that the killer circuit turns on when the unit is in SECAM reception mode, so that the signals available at pins ㊻ and ㊽ are cut off not entering the demodulator circuit.

For output DC voltage of pin ① and pin ②, its temperature characteristic is designed to be nearly zero. To complement this, the video output (pin ⑤) has the temperature characteristic equivalent to $2V_{BE}$, finally making zero the DC voltage temperature characteristic of each of R, G and B output signals. Here must be used a low pass filter to meet the generation of high frequency component.

POWER SUPPLY REGULATOR CIRCUIT

The power supply control circuit of this model is of the primary and secondary side separation type, which uses switching regulator circuitry. The main elements are enclosed in a flat package, and the supply voltage is factory-set. The major features include:

1) Double insulation structure completely separetes the primary and secondary sides for the so-called "cold chassis".
2) Number of parts is greatly reduced, resulting in improved reliability.
3) No supply voltage setting is needed.
4) The main circuits are contained in a single package, making replacement easy if required.
5) Two ways of operational mode are available; standby and full-power operation.
6) The input voltage is widely controllable between 90 and 280V.

Operation

The main parts of the circuit are shown on page 30 where the power supply regulator IC is enclosed with the broken line. The function of each component is as follows:

Q1 : error detection amplifier
Q2 : drive stage
Q3 : control switch transistor
ZD1 : zener diode for comparison
Q702: off lock switch transistor
Q701: over-current limiter
D711: trigger diode
D705: pulse clipper
D708: detection voltage rectifying diode
D732: +B (≒ 115V) rectifying diode
D733: +B (≒ 12V) rectifying diode
D301: audio power supply rectifying diode

The actual operation is as follows:

Standby mode

1) With the power (MAINS) switch on, the AC input voltage is rectified by D701 and C707. (B_0 = 280V DC at AC 220V).
   At this time, both Q1 and Q2 remain off. Accordingly, current i_1 flowing through R711 and C714 directly enters pin ② of IC701 to change into Q3 base current i_B.
2) The Q3 base current i_B causes the collector current i_2 to start flowing. That is, the current starts to flow from pin ② of the regulator transformer T701 towards pin ⑦. This current generates drive voltage e_0 between pins ③ and ④ of transformer T701, causing drive current i_3 to start flowing and increasing the Q3 base current i_B.
   Consequently as current i_B increases, current i_2 becomes greater, thus turning Q3 abruptly on.
3) When Q3 is completely saturated, it does not act to amplify the current, and i_2 stops increasing and the generation of e_0 is discontinued. Therefore, i_3 goes out and Q3 turns off.
4) The instant that Q3 turns off, the magnetic energy stored between pins ② and ⑦ of transformer T701 is fed out of pins ⑪ and ⑫ of the same transformer. This energy is rectified by L731, D732 and C731 to allow current i_D into the secondary load.
5) When the magnetic energy all flows out to the secondary side, the secondary side turns off and at the same moment the primary side (Q3) turns on.
   By this automatic oscillation (blocking oscillation), the secondary output voltage gradually rises.
6) As the secondary output voltage becomes greater, the voltage induced at the coil at pins ④ and ⑤ of transformer T701 is also rising. R1, R2 and ZD1 have been determined so that Q1 turns on when the induced voltage has reached a preset level.
   Now when Q1 turns on, the base current i_6 of Q2 flows to activate Q2. Then the current i_C flows to absorb the base current i_B of Q3.
7) When the secondary output voltage B_1 rises, the voltage between pins ④ and ⑤ of transformer T701 also in creases. This causes Q1 and Q2 to turn on, the base current of Q3 to decrease, and the off time to be prolonged. When the off time of Q3 is longer, the magnetic energy stored in the primary coil (between pins ② and ⑦) of transformer T701 becomes less, causing the secondary output voltage B_1 to decrease.
8) To the contrary, when the secondary output voltage B_1 becomes lower, Q1 and Q2 turn off, the base current i_B increases and the on time is prolonged. Which means the voltage B_1 comes higher. Thus the secondary output voltage B_1 is kept constant.
9) The off clock circuit consists of Q702, R742, R743, C725, D715 and T701 (pins ④ and ⑥). Q702 is intended to absorb part of i_3 to cut down half the frequency of the self-excited oscillator.
   This design provides less power loss at the primary circuit.

Full-power operation

1) By turning on the remote control unit in the standby mode, the secondary load abruptly becomes great.
2) At this time, the horizontal circuit at the secondary side starts operation, generating the FBT pulse at the FBT (pins ⑪ and ⑫). This signal flows through D711 and R729, allowing trigger current i_4.
3) The current i_4 is combined with drive current i_3 into current i_5, which is fed to pin ② of the IC. Now the oscillation of Q3 is synchronized with the horizontal frequency of trigger current i_4.
4) The secondary output voltage B_1 is controlled in the same way as in the standby mode.
   The +B (≒ 12V) output and the audio output are also controlled the same manner as the output B_1 which was discussed earlier with respect to pins ⑪ and ⑫ of transformer T701.

A pulse clipper circuit and an over-current limiter circuit are peripherally attached to this circuit. The pulse clipper circuit consists of R723, C708 and D705. It protects Q3 by cutting off the part of the voltage higher than the specified level because the collector voltage of Q3 rises high for a moment when Q3 turns off.
The over-current limiter circuit consists of Q701 and R705. It protects Q3 against possible damage due to a large current (collector current).

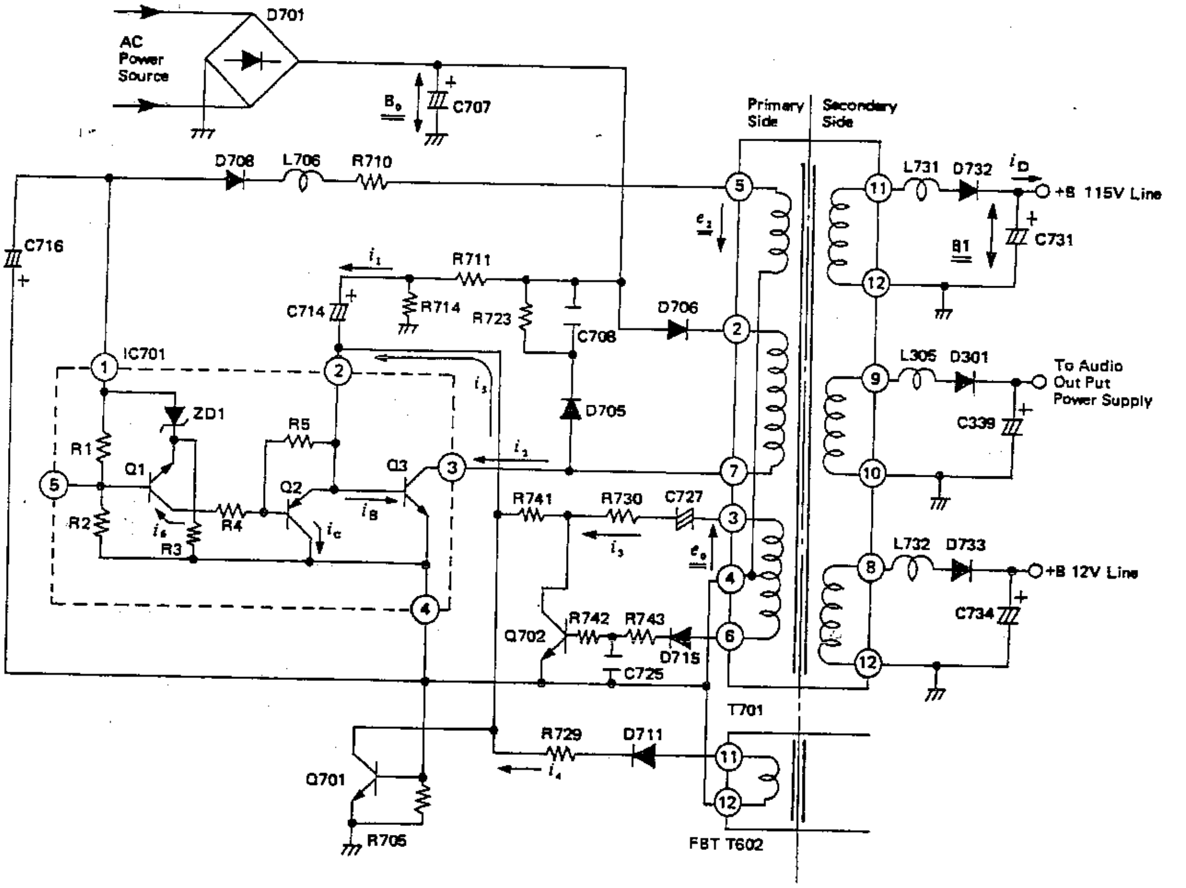
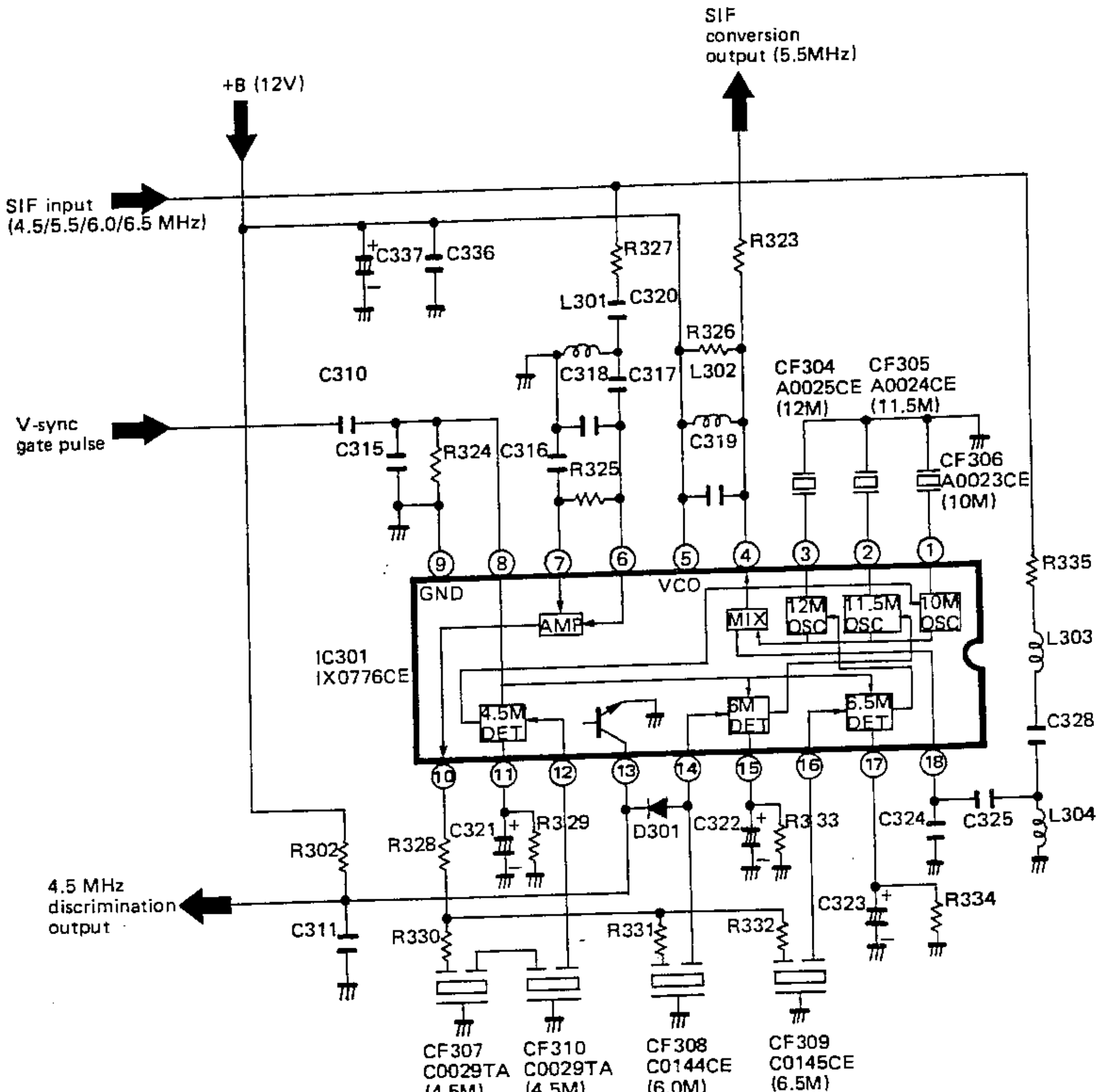


Figure 46. Power Supply Regulator Circuit

SIF DISCRIMINATION AND CONVERTER CIRCUITS



Conditions at pin 13	13 PIN
4.5MHz SIF input	L
Others	H

Output at pin 13 ; open collector

Received signal	Audio carrier wave frequency
SYSTEM M	4.5 (MHz)
SYSTEM B/G	5.5 (MHz)
SYSTEM I.	6.0 (MHz)
SYSTEM D/K	6.5 (MHz)

Figure 47. SIF Discrimination and Converter Circuits

From the PIF/SIF IC (pin 10 of PIF PACK), the SIF signal (4.5/5.5/6.0/6.5 MHz) corresponding to the reception mode flows into pin 6 (SIF discrimination input) and pin 18 (SIF mixer amplifier input) of IC301.

The signal coming into pin 6 is internally subjected to the limiter and the amplifier, and goes out of pin 10.

This outgoing signal from pin 10 passes through the 4.5 MHz, 6.0MHz and 6.5MHz filters and the resultant signals are fed into pins 12, 14 and 16, respectively, and again internally detected.

When the SIF signal frequency is 4.5 MHz, pin 12 becomes high level and the 10 MHz signal is oscillated at pin 1. When it is 6.0 MHz, pin 15 becomes high level and the 11.5 MHz signal is oscillated at pin 2.

In the case of 6.5MHz, pin 17 becomes high level and the 12MHz signal is oscillated at pin 3.

Moreover, these SIF signals are mixed into the 5.5MHz signal, which goes out of pin 4. If the SIF signal frequency is 5.5MHz initially, the signal is amplified at pin 18 and goes out of pin 4.

RECEPTION SINGAL SYSTEM DISCRIMINATOR CIRCUIT

The System discriminator circuit is an integrated circuit which consists of 4.5 MHz discriminator, 50 Hz/60 Hz discriminator, PAL discriminator and their peripheral logic circuit.

Fig. 48 shows a block diagram of this system discriminator IC (RH-iX0354CEZZ), and Table 7 represents how the pin condition of the IC changes according to the systems of TV signals in ereception.

Table 7. Pins Conditions of IC (RH-iX0354CEZZ) Depending On the Systems of TV Signals in Reception.

Reception signal						Input pin			Output pin					
						22	23	26	10	11	12	13	20	21
	—	CHROMA (MHz)	SIF (MHz)	VERTICAL HZ	HORIZONTAL (kHz)	SECAM Killer	P/N killer	PAL DET	B.P. X-Tal	PIF/S	V	H	P/N switch	ARC switch
1	CCIR-B/G PAL	4.43	5.5	50	15.625	L	H	H	H	L	L	L	L	L
2	CCIR-B/G SECAM	4.25/4.406	5.5	50	15.625	H	L	L	H/L	L	L	L	L	L
3	OIRT-D/K PAL	4.43	6.5	50	15.625	L	H	H	H	L	L	L	L	L
4	OIRT-D/K SECAM	4.25/4.406	6.5	50	15.625	H	L	L	H	L	L	L	L	L
5	CCIR-M NTSC	3.58	4.5	60	15.734	L	H	L	L	H	Hz	Hz	Hz	H
6	CCIR-I PAL	4.43	6.0	50	15.625	L	H	H	H	L	L	L	L	L
	[VTR]													
7	NTSC-4.43	4.43	5.5	60	15.734	L	H	L	H	L	Hz	Hz	Hz	L
8	NTSC-3.58-5.5	3.58	5.5	60	15.734	L	H	L	L	L	Hz	Hz	Hz	H
	[VIDEO DISC]													
9	PAL-DISC	4.43	5.5	60	15.625	L	H	H	H	L	Hz	L	L	L
10	NTSC-DISC	3.58	4.5	50	15.734	L	H	L	L	H	L	Hz	Hz	H
11	SECAM-DISC	4.25/4.406	5.5	60	15.625	H	L	L	H/L	L	Hz	L	L	L

Note 1:
Video disc in use:
PAL-DISC; When NTSC disc is played with a PAL disc player.
NTSC-DISC; When PAL-SECAM disc is played with an NTSC disc player.
SECAM-DISC; When NTSC disc is played with a SECAM disc player.

Note 2:
H : High level
L : Low level
Hz: Open collector

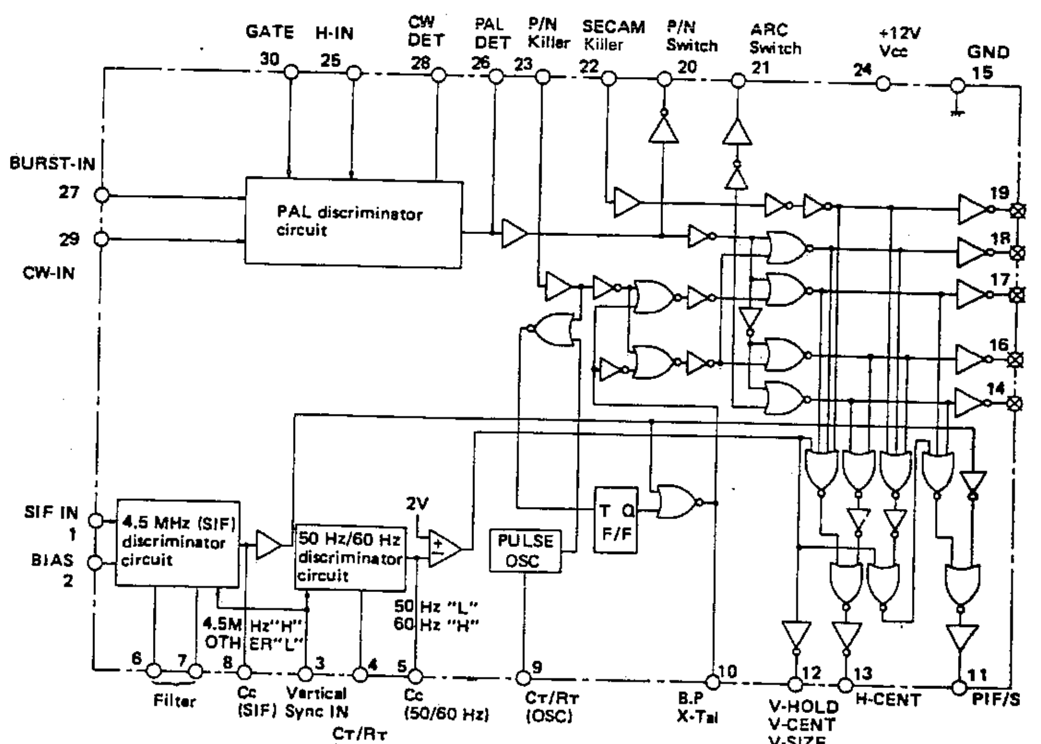


Figure 48. Block Diagram of System Discriminator IC

DESCRIPTION OF ELEVEN COLOR TELEVISION SYSTEMS

Generally speaking, there are three important color systems in the world, i.e. PAL system SECAM system and NTSC system, and they are further divided into 16 systems as follows, the details of each of which are shown in Table 8 .

1. PAL-B
2. PAL-G
3. PAL-I
4. PAL-N
5. PAL-M
6. PAL-60
7. SECAM-B
8. SECAM-G
9. SECAM-D
10. SECAM-K1
11. SECAM-L
12. SECAM-60
13. NTSC-M
14. NTSC-N
15. NTSC-50
16. PAL-D

This unit is able to receive eleven color television systems out of the sixteen, which are shown below.

① PAL-B/G
② PAL-I
③ PAL-60
④ SECAM-B/G
⑤ SECAM-D/K1
⑥ SECAM-60
⑦ NTSC-M
⑧ NTSC-50
⑨ PAL-D

When in VTR playback mode, this unit can receive the following two systems.

⑩ NTSC 4.43−5.5
⑪ NTSC 3.58−5.5

Table 8.

Item \ Television system	PAL system						SECAM system						NTSC system		
Formal name	PAL-B	PAL-G	PAL-I	PAL-N	PAL-M	PAL-60	SECAM-B	SECAM-G	SECAM-D	SECAM-K1	SECAM-L	SECAM-60	NTSC-M	NTSC-N	NTSC-50
Popular name (by RF)	B	G	I	N	M	—	B	G	D	K1	L	—	M	N	—
Geographical name	CCIR (West European) system		British system	Argen-tine system	Brazilian system	VHD system	Middle and Near East system		OIRI (East European) system		French system	VHD system	U.S.A. system	—	VHD system
Broadcast channel	VHF	UHF	VHF & UHF	VHF	VHF & UHF	UHF	VHF	UHF	VHF	UHF	UHF	UHF	VHF & UHF		VHF & UHF
Number of scanning lines	625				525		625					525	525	625	
Field frequencies	50 Hz				60 Hz		50 Hz					60 Hz	60 Hz	50 Hz	
Line frequencies	15.625 kHz				15.734 kHz	15.625 kHz	15.625 kHz						15.734 kHz	15.625 kHz	15.734 kHz
Colour subcarrier frequencies	4.43 MHz			3.58 MHz		4.43 MHz	4.25 MHz/4.40 MHz						3.58 MHz		
(Audio)–(Video)	5.5 MHz		6 MHz	4.5 MHz		4.5, 5.5, 6 MHz	5.5 MHz		6.5 MHz				4.5 MHz		
	Italy Austria Holland Sweden West Germany Norway Portugal Denmark Switzerland Spain Finland Sri Lanka.....		Ireland (VHF) England (UHF) South Africa Hong Kong (UHF)	Argenting Uruguay Paraguay	Brazil	PAL VHD Disc play-er at Play mode	Saudi Arabia Libya Greece East Germany		U.S.S.R. Hungary Poland Monogolia Czechoslovakia		France Monaco Luxemburg	SECAM VHD Disc player at play mode	U.S.A. Hawaii Ecuador Canada, Mexico Guatemala Costa Rica Columbia Chile, Cuba Dominica Japan	None	NTSC VHD Disc player at play mode
	Algeria Kuwait Liberia Pakistan India						Iran Iraq Lebanon		Bulgaria Romania (Black & white) Congo (Black & white) China (PAL-D)	Tahiti (VHF) Gabon (VHF) Ivory Coast (VHF) Zaire (VHF) Togo (VHF) New Caledonia (VHF)					

TV/AV SELECTOR CIRCUIT

Selection of the TV and AV modes is controlled according to the voltage from the microprocessor in the transmitter. Figure 49 depicts the block diagram of the TV/AV selector circuit.

The flow of the video signal is described first. At pin ⑮ of PIF PACK is detected and delivered the signal from the RF-ANT input terminal (composite video signal). This signal is applied to the base of Q440 through the high-frequency and sound carrier filters first and then sent to the video switching IC (IC1402, pin ②) through the emitter-follower. On the other hand, the video signal from the external video input terminal goes through the buffer amplifier Q1403 for level adjustment and enters IC1402 at pin ⑦. These two video signals that have entered IC1402 are controlled by the voltage at pin ③ and either of them is developed at pin ④. The video signal delivered at pin ④ goes through the buffer amplifier Q1401 and the 4.5 MHz trap filter (CF1401), arriving at pin ⑦ of IC1401. On pin ② of IC1401 is impressed an unfiltered video signal. IC1401 is a 4.5 MHz filter switching IC. Its function is to switch the 4.5 MHz trap according to the broadcasting system of the selected broadcasting station when a signal is received through the RF-ANT input terminal. If the broadcasting system of the selected broadcasting station is SYSTEM-M (sound carrier = 4.5 MHz), this IC allows a received signal to go through the 4.5 MHz filter; and if not, it prevents any received signal from passing through that filter. This switching operation is controlled by the voltage developed at pin ③. The filtered or unfiltered video signal is delivered at pin ④.

The output signal at pin ④ is sent to the video/chroma/sync circuit as well as the video output amplifier circuit composed of Q1405 and Q1406 for level and frequency correction and then outputted from the external video output terminal.

For the audio signal, the audio signal component of the RF-ANT input signal from pin ⑧ of PIF PACK and the audio signal from the external audio input terminal are applied to pin ② and pin ⑦ of IC1303, respectively, and the output of the audio signal at pin ④ is controlled by the voltage at pin ③. The audio signal developed at pin ④ is sent to the audio attenuator IC (IC1302) as well as the audio output amplifier circuit composed of Q1305 and Q1306 for level adjustment. Then the signal is outputterd from the external audio output terminal.

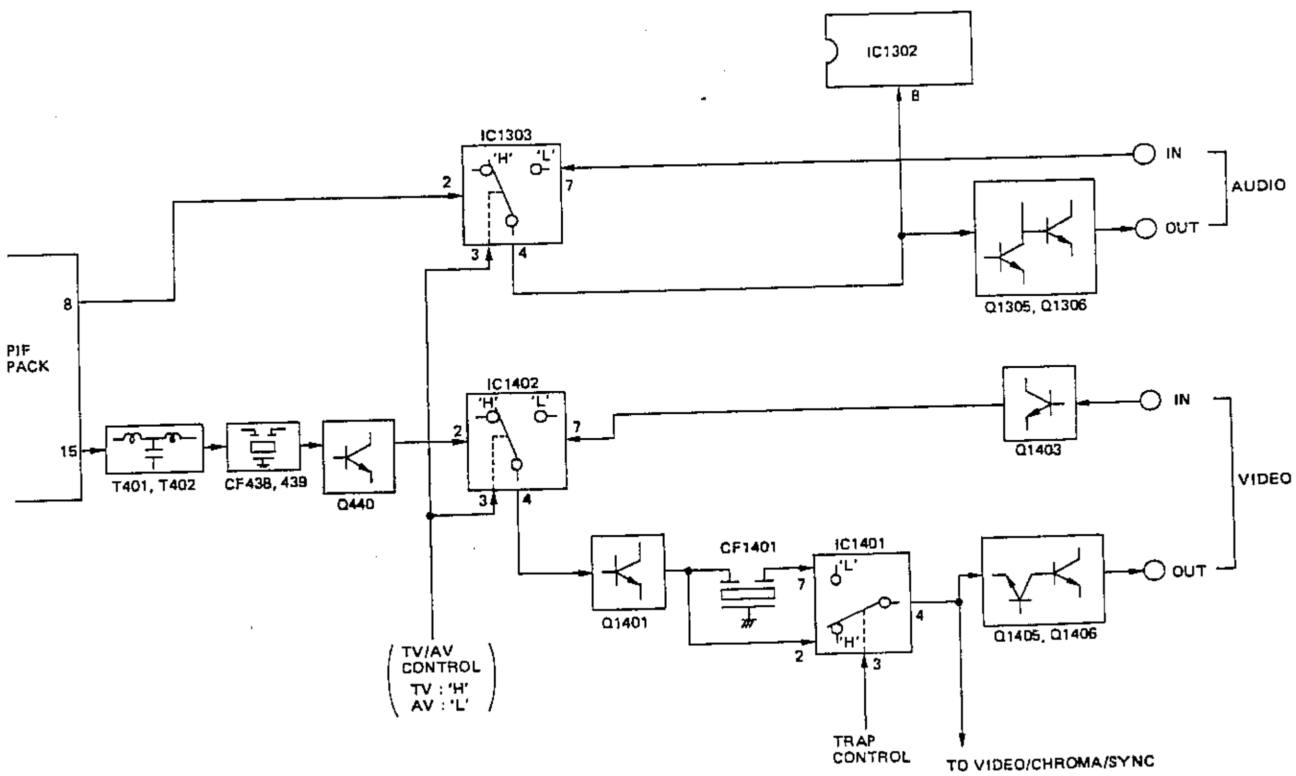


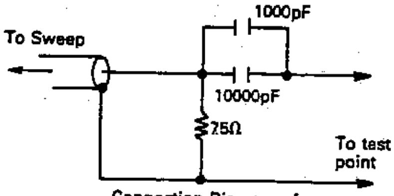
Figure 49.

SERVICE ADJUSTMENT
PIF/AFT/SIF/AGC ADJUSTMENT

Tuner IFT coils:

* The tuner has been factory preset (no adjustment is needed).

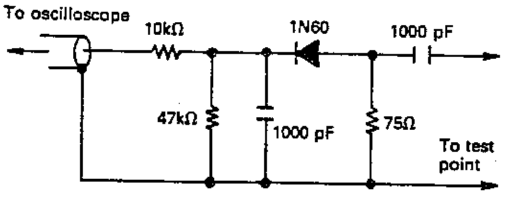
1. Set reception channel at E10CH (When such signal is not available, set VT voltage at 5V in VIII band.)
2. Connect sweep generator's output ot the test point of tuner, by using a 75Ω DC cut probe.



Connection Diagram of 75Ω DC Cut Probe

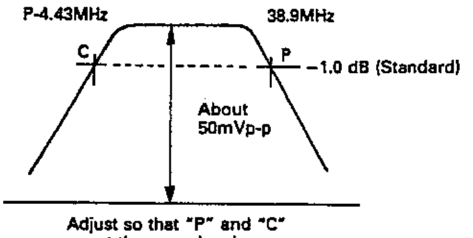
*Note:
The sweep generator's prove should be grounded closely to the tuner test point.

3. Output level of sweep generator: 80 dB
4. Connect response lead (low impedance probe with detector) to the collector of Q201 (in IF pack).



Connection Diagram of Low Impedance Probe (with Detector)

5. PIF AGC:
   Apply DC 3V to pin ④ of IF pack.
6. RF AGC:
   Apply DC 4V to the tuner AGC terminal.
7. Adjust the tuner IF coils to obtain the waveform as shown figure below.



Adjust so that "P" and "C" are at the same level.

P-detector coil: T204

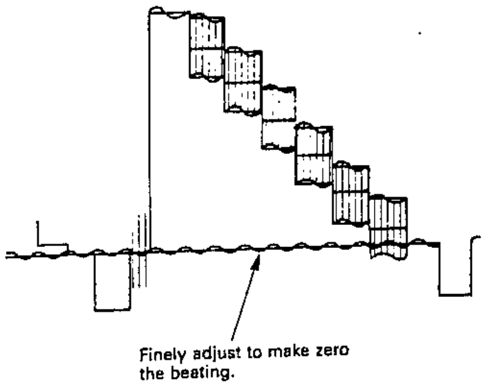
* This coil (in IF pack) has been factory preset (no adjustment is needed).

1. Connect signal generator to pin ⑨ of IC201 (in IF pack).
   Generator output: 90dB
   Modulation: CW (38.9 MHz)
2. Connect digital voltmeter of oscilloscope to TP401.
3. AGC:
   Apply DC voltage to pin ④ of IF pack. Adjust AGC so that voltage at TP401 becomes about DC 4V.
   Note: Voltage applied to AGC should not exceed DC 7V.
4. Adjust T204 to obtain minimum DC voltage at TP401.
   Note: At the end of the adjustment, see that there is about DC 4V at TP401. If not, readjust AGC and T204.

AFT coil: T203

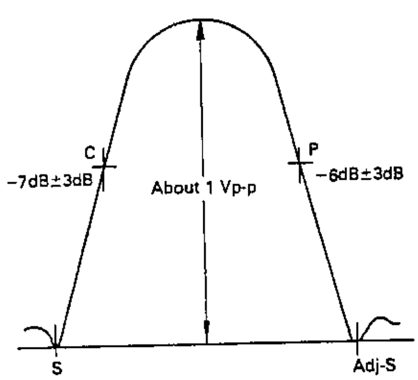
* This coil (in IF pack) has been roughly preset in the factory.

1. Receive E12CH signal (PAL colour bar signal).
   If E12CH signal is not available, it is enough to receive the signal of more than E5CH or UHF signal).
   - Signal strength: Over 55dB, Below 80dB
2. Connect oscilloscope to pin ③ of (FT) connector.
   - Oscilloscope range: 0.5V/DIV
   - Sweep time: 20μsec/DIV
   - Synchronization: Horizontal sync
3. Connect the output of SSG (Standard Signal Generator) to the tuner IF output terminal or pin ① of (FT) connector across a capacitor of 1PF.
   - SSG output: 38.9 MHz ± 5 kHz (non modulated)
   - SSG output level: about 50 dB
   * When the preset switch is set to U or V position, and the FINE key is pushed, AFT is turned off.
   * When the preset switch is set at NORMAL postion, AFT is turned on.
   With the switch at NORMAL position, however, AFT becomes turned off if FINE button of tuning control is pushed. (Channel character on screen is displayed yellow.)
4. Set the preset switch at V position and adjust FINE button (Up or Down) of tuning control so that the output waveform suffers no beating.
5. Set the preset switch at NORMAL position.
6. Adjust T203 so that no beating is caused at the output waveform.



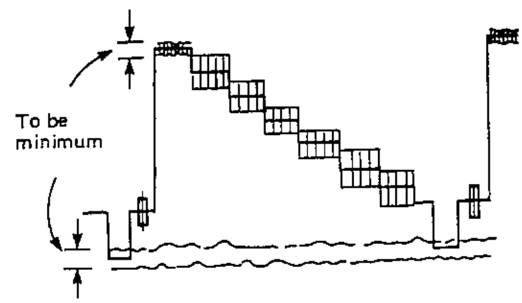
PIF overall waveform

1. Receive E10CH signal.
   If E10CH signal is not available, set VT voltage at 5V in VIII band.
2. Connect sweep generator's output to the test point of tuner.
- Probe in use: 75Ω DC cut probe
- Sweep output level: 70 dB
3. Connect response lead to TP401.
   The response lead in use should be a direct probe with a resistor of 10 kohms included.
4. RF AGC:
   Apply about 4V DC to the tuner AGC terminal.
5. PIF AGC:
   Apply about 5V DC to pin ④ of IF pack.
6. Connect a 120 ohm damping resistor between pins ㉖ and ㉗ of IC201 (in IF pack).
7. Turn off AFT.
   AFT is turned off is pin ⑫ of IF pack is grounded.
8. Adjust IF AGC voltage so that the output waveform is of about 1Vp-p.
9. Check that the overall waveform is as shown in Figure below.



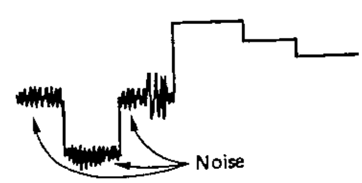
NTSC 4.5 MHz trap: T201

1. Receive NTSC 3.58 MHz colour bar signal.
   Signal strength: 55−80 dB
2. Connect the oscilloscope probe to pin ③ of (FT) connector.
   Voltage range: 0.5V/div.
   Sweep time: 20μsec/div.
   sync method: Horizontal
3. Adjust T201 so that the oscilloscope waveform's 920 kHz beat be minimum.



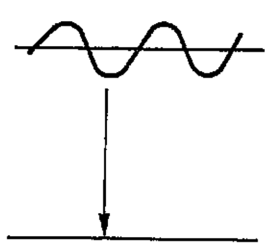
RF AGC cut-in control: R218

1. Receive "PAL colour bar" signal.
2. Field intensity: 75 dB
3. Connect oscilloscope to TP401 (with horizontal sync signal).
4. Turn R218 (AGC control) to the position where noise appears on oscilloscope.
5. Slowly turn back R218 until noise disappears. AT the time, the output of horizontal sync signal should not be reduced.
6. Change the field intensity to 90 dB and see that there is no cross modulation and beating on oscilloscope.
7. Change the field intensity to 60 dB and see that there is no noise on oscilloscope.



SIF detector coil (5.5 MHz): T301

1. Apply AGC voltage (DC3V) to pin 2 of IC201 (in IF pack).
2. Make maximum RF-IN Sub-Sound (R301)
3. Apply signal generator output to the IC301 pin 4.
   - Frequency: 5.500 MHz
   - Modulation: 400 Hz, AM 30%
   - Generator output: 74 dB
4. connect oscilloscope to TP342.
   Range: 50mV/div.
5. Adjust T301 so that sound signal (AM 400 Hz) on oscilloscope becomes minimum.



RF-IN Sub-Sound: R301

1. Connect pattern generator to the receiver, and receive "PAL colour bar" signal (at sound modulation 400 Hz 100%).
2. Connect oscilloscope to TP342.
3. Adjust R301 so that the output waveform is of 0.75 Vp-p.

Sub-Sound: R1313

1. Connect pattern generator to the receiver, and receive "SECAM colour bar" signal (at sound modulation 400 Hz 60%).
2. Connect oscilloscope to TP301.
3. Adjust the volume control to have the maximum sound output.
4. Adjust R1313 to the point where the output waveform just begins to be distorted.

VIDEO/CHROMA ADJUSTMENT

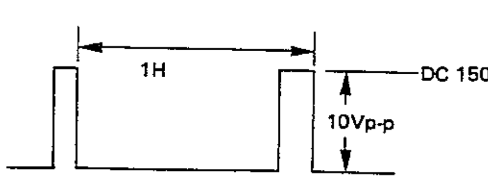
CRT cut-off and Sub-Brightness adjustment

- R853: R-bias control
- R859: G-bias control
- R865: B-bias control
- Screen control
- R857: G-drive control
- R863: B-drive control
- R422: Sub-Brightness control

*Note:

Prior to this adjustment, warm up the unit with the beam current of more than 700μA for more than 30 minutes.

1. Receive monoscope pattern signal.
2. Set R857 at CENTER position.
   Set R863 at CENTER position.
   Set R853 at MIN position.
   Set R859 at MIN position.
   Set R865 at MIN position.
3. Set the screen control at MIN position.
4. Set the Brightness control at center click position.
5. Connect the oscilloscope probe to TP852 (red cathode).
6. Turn on S401 (service switch).
7. Adjust Sub-Brightness control (R422) so that the output waveform is 10Vp-p.



8. Slowly turn the screen control clockwise until the horizontal raster appears slightly, and stop it.
9. Here, one of the three colours (red, green, blue) appears first as the screen control is turned. So, touching off the bias control belonging to the first colour, use and move the other two controls so that the horizontal raster becomes white.
10. Turn the screen control counterclockwise until the horizontal raster disappears, and stop it.

White balance and back ground

- R857: G-drive control
- R863: B-drive control
- R407: Sub-contrast control

*Note:

Prior to this adjustment, warm up the unit with beam current of more than 700μA, for more than 30 minutes.

1. Receive monoscope pattern signal.
2. Set the contrast control and brightness control at MAX postion.
3. Connect beam ammeter to TP601 and TP602.
   (Full scale: 3mA)
4. Adjust R407 so that the beam current becomes 0.8mA (rough adjustment).
5. Set the contrast control at the MAX position with the use of R/C transmitter.
6. Adjust R857 and R863 so that the colour temperature is at 11500°K. (High beam: 0.8mA)

7. Adjust the contrast control and brightness control so that the beam current is about 200μA, and check that the colour temperature is at 11500°K. If the temperature is not at 11500°K, go back to "CRT cut-off adjustment" and repeat the adjustment.

Sub-contrast control: R407

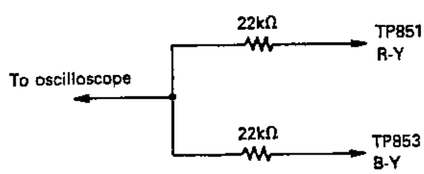
*Note:
Prior to this adjustment, warm up the unit with beam current of more than 700μA, for more than 30 minutes.

1. Receive monoscope pattern signal.
2. Set the contrast control and brightness control at MAX position.
3. Connect beam ammeter to TP601 and TP602. (Full scale: 3mA)
4. Set the contrast control at the MAX position with the use of R/C transmitter.
5. Adjust R407 so that the beam current becomes 0.8mA.

PAL chroma adjustment

R823: 1H-delay amp control
T802: 1H-delay phase control
T803: CW phase control

1. Receive PAL colour bar signal.
* Before this adjustment, the PIF/AFT/AGC adjustment must have been completed.
2. Connect the following resistance matrix to TP851 and TP853, to which an oscilloscope is connected.



Resistance Matrix

3. Set the contrast control and brightness control at MAX position.
4. Adjust the colour control so that the output waveform of colour difference signal becomes 1.5Vp-p.
5. Adjust R823, T802 and T803 so that the output waveform shown in Fig. a is corrected to that shown in Fig. b.
6. Set the contrast control and colour control at the NEUTRAL position with the use of R/C transmitter.

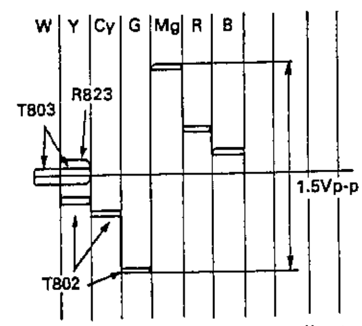


Figure a. Waveform before the adjustment

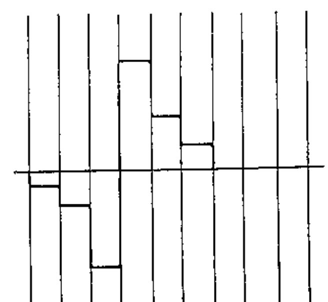
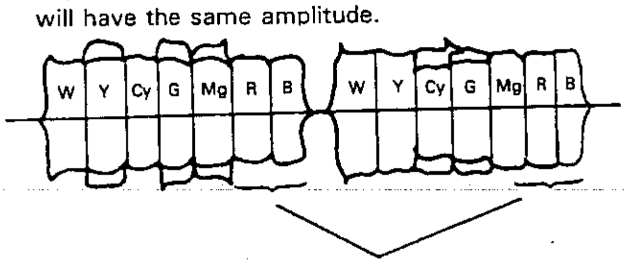


Figure b. Waveform after the adjustment

SECAM ADJUSTMENT

Bell filter adjustment: T931

1. Receive "SECAM colour bar" signal.
2. Connect oscilloscope to TP931.
   Range: 0.05V/cm AC
   Scan time: 20μsec/cm
   Probe: 1/10 (30 pF/10 MΩ or more)
3. Adjust T931 so that the read output and blue output will have the same amplitude.

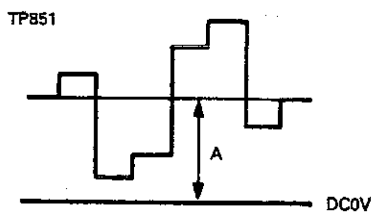


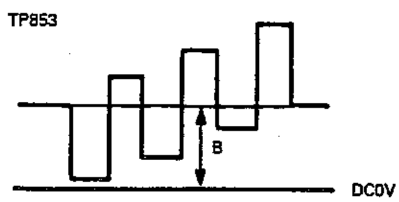
Killer adjustment: T934

1. Receive "SECAM colour bar" signal.
2. Connect oscilloscope TP932.
   Range: 1 V/cm DC
   (Adjust V-position.)
   Scan time: 20μsec/cm
3. Adjust T934 to obtain maximum DC voltage (about 9.5V).

R-Y (T933), B-Y (T932) discriminator

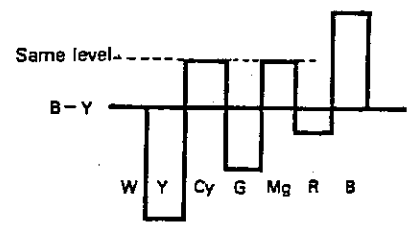
1. Receive "SECAM colour bar" signal.
2. Connect oscilloscope to TP851 (R-Y) and the TP853 (B-Y).
   Range: 2 V/cm DC
   Scan time: 10μsec/cm
3. Set contrast control and brightness control at MAX position.
* Connect capacitor (0.001μF) to TP851 and TP853, thus to prevent noise interference.
4. Adjust T933 (R-Y) and T932 (B-Y) so that DC output level with colour control set at MIN will be the same as that with colour control set at as that with colour control set at 100% of saturation.





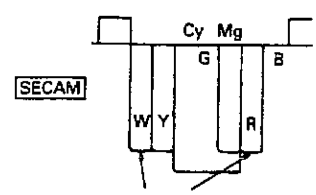
NTSC HUE: T801

1. Receive pattern generator signal of NTSC 4.43 MHz.
2. Connect oscilloscope to TP853 (B-Y).
3. Set contrast control at NORMAL position.
4. Set brightness control at CENTER position.
5. Turn colour control to obtain the output of about 3Vp-p.
6. Adjust R837 (hue control) so that the output waveform is as shown in figure below.
7. After adjusting R837 (hue control), receive pattern generator signal of NTSC 3.58 MHz.
8. Adjust T801 so that the output waveform is as shown in figure below.



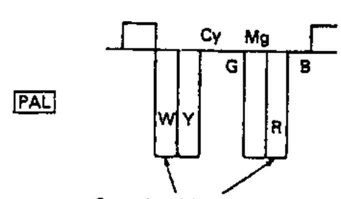
Sub-colour adjustment: R814

1. Receive "SECAM colour bar" signal.
2. Set contrast control at the MAX position.
3. Set brightness control at the MAX position.
4. Connect oscilloscope to the TP852 (Red output).
5. Adjust the colour control so that saturation of 100% is obtained.
6. For SECAM colour bar signal reception, adjust Colour control so that the white output (75%) and red output will have the same level.



Same level for the white and red outputs.

7. Receive "PAL colour bar" signal.
8. For PAL colour bar signal reception, adjust R814 so that the white output (75%) and red output will have the same level.



Same level for the white and red outputs.

ADJUSTMENTS OF SYNC AND DEFLECTION CIRCUITS

H-frequency adjustment: R606

1. Connect pattern generator to the receiver, and receive "standard PAL or SECAM colour bar" signal.
2. Short pin ㉖ of IC801 and 12V line.
3. Adjust R606 for good horizontal sync.

V-Hold adjustment: R511

1. Connect pattern generator to the receiver, and receive "standard PAL or SECAM colour bar" signal.
2. Turn R511 (V-hold control) until vertical sync will be proper.

H-size tip

1. Connect pattern generator to the receiver, and receive "standard crosshatch colour bar" signal.
2. Insert H-size tip to the position where H-size will be best.
   H-size: 8% (10% max.)

V-size and V-line adjustment

- R506: V-size
- R518: V-line

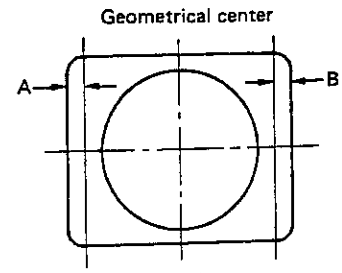
1. Receive PAL crosshatch pattern signal.
2. Adjust R506 and R518 so that the output pattern will be best.
   V-size: 8% (10% max.)
   V-line: 0 ± 5%

Sub-V-size: R516

1. Receive NTSC crosshatch pattern signal.
   V-frequency: 60Hz
2. Adjust R516 to have V-size be at 8% of overscanning.

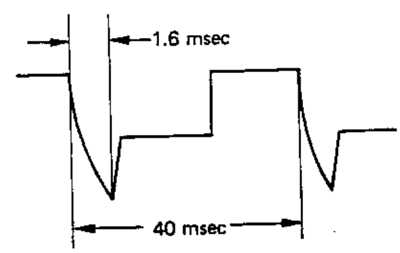
H-cent: R611

1. Receive PAL or SECAM crosshatch pattern signal.
2. Adjust R611 so that the picture's horizontal center is A = B.



50 Hz Pulse width adjustment: R1807

1. Receive standard PAL crosshatch pattern signal.
2. Connect oscilloscope to TP1802.
3. Adjust R1807 to obtain the pulse width of 1.6 msec.



PURITY ADJUSTMENT

Purity adjustment

1. Prior to the purity adjustment, warm up the unit with beam current of more than 700μA, for more than 30 minutes.
2. Receive the green signal alone and adjust the beam current to about 700μA.
3. Fully degauss the CRT with the degaussing coil.
4. Before the purity adjustment, it is needed to roughly adjust the static convergence.
5. Set the purity magnet at the position which gives zero (0) magnetic field.

Adjustment:

- During the adjustment, keep the unit facing the east.

6. Observe the green spots ("a" and "b") with a microscope as shown in Fig. A, and adjust the purity magnet so that they are at the specified landing position.

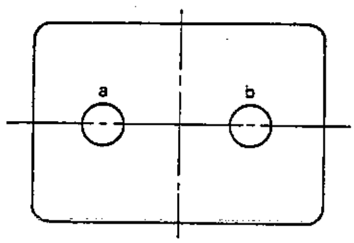
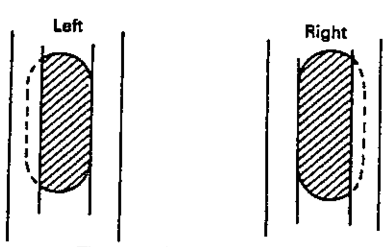


Figure A

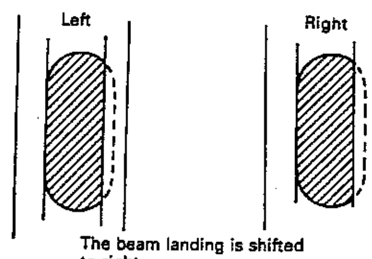
7. If the right and left green spots are both deviated outwards from their landing positions as shown in Fig. B push the deflection yoke forwards until their positions are corrected.



The beam landing is shifted outwards.

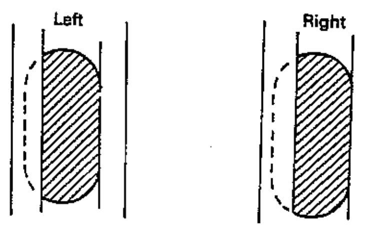
Figure B

8. If the beam landing is shifted to right or to left as shown in Figs. C and D, adjust the opening degree of the purity magnet so that the beam landing is correctly positioned.



The beam landing is shifted to right.

Figure C



The beam landing is shifted to left.

Figure D

9. Adjust the purity magnet so that the beam landing is correct at either of the centeral part, right and left parts of screen, then check that the green beams at four corners of screen are all correctly positioned. Finally, check that the beam landing at any pat of screen is satisfactory with the Rank "B" specifications.
10. If the green beam is positioned to mix with the other colour, pull the deflection yoke backward.

- Outside of the specified landing: To front of the deflection yoke
- Inside of the specified landing: To back of the deflection yoke

11.Set the raster rotation at "0" position (with the unit fasing the east.)

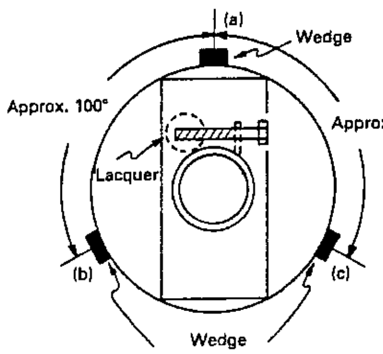
12.Tighten the screws of the deflection coil.
Tightening torque: 11kg±2kg

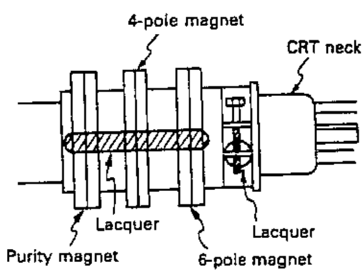
CONVERGENCE ADJUSTMENT

Convergence adjustment

This adjustment should be performed after the purity magnet adjustment.

1. Receive crosshatch pattern signal.
2. Set the brightness control and contrast control at MAX position.





- Static Convergence

3. Adjust the opening degree of the 4-pole magnet and rotate the magnet to converge red and blue lines.
4. Adjust the opening degree of the 6-pole magnet and rotate the magnet to converge red, blue and green lines.

- Dynamic convergence

5. Dynamic convergence (convergence of the three colour fields) at the edges of CRT screen is accomplished in the following manner.

- Convergence in Fig. a:
  Insert wedge (a) between the deflection yoke and CRT, and tilt the deflection yoke upward until the mis-convergence shown in Fig. a is corrected.

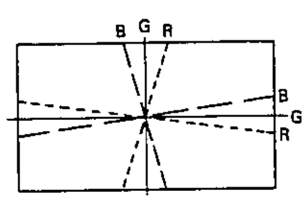


Figure a

- Convergence in Fig. b:
  Insert wedges (b) and (c) between the deflection yoke and CRT, and tilt the deflection yoke until the mis-convergence shown in Fig. b in corrected.

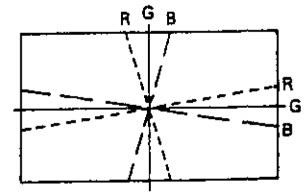


Figure b

- Convergence in Fig. c:
  Insert wedge (c) deeply between the deflection yoke and CRT, and tilt the deflection yoke to right until the mis-convergence shown in Fig. c is corrected.

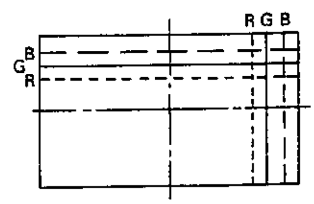


Figure c

- Convergence in Fig. d:
  Insert wedge (b) deeply between the deflection yoke and CRT, and tilt the deflection yoke to left until the mis-convergence shown in Fig. d is corrected.

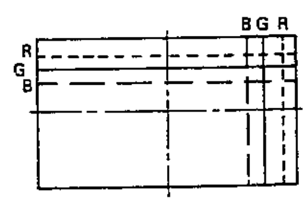


Figure d

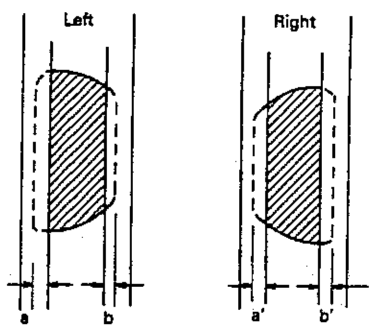
6. Stick the three wedges onto the CRT, and apply glass tapes thereon.
7. Apply lacquer to the deflection yoke screw, magnet unit (made of purity, 4-pole and 6-pole magnets) and magnet unit screw.

After the adjustment, receive either the Red or the Blue signal and check that there is no mixture with the other colour signal.

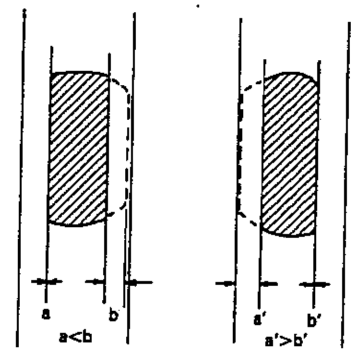
CAUTIONS ON LANDING ADJUSTMENT

CRT landing

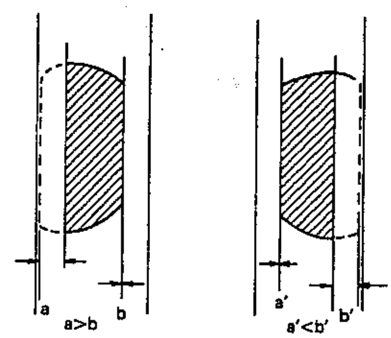
Fig. E shows the good landing of, beams on CRT, in which a=b and a'=b' are established. In this condition, the lighting beam has a trapezoidal form.



Good Landing Rank A
Figure E



Not Good Landing Rank B
Figure F



Not Good Landing Rank B
Figure G

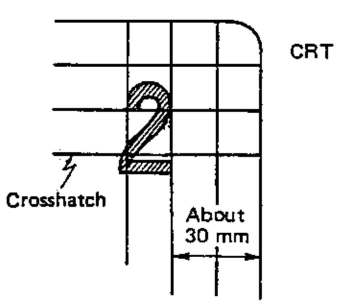
- Cautions on the adjustment:

1. When the good landing is obtained as shown in Fig. E, the lighting beam is hard to be mixed with the other beam even with positional change of the purity magnet.
   However, if the landing is not good as shown in Fig. F and G, the mixture of two beams is likely to occur with positional change of the purity magnet.
2. If the landing is poorly adjusted as shown in Figs. F and G, there will be a problem of doming of beams.

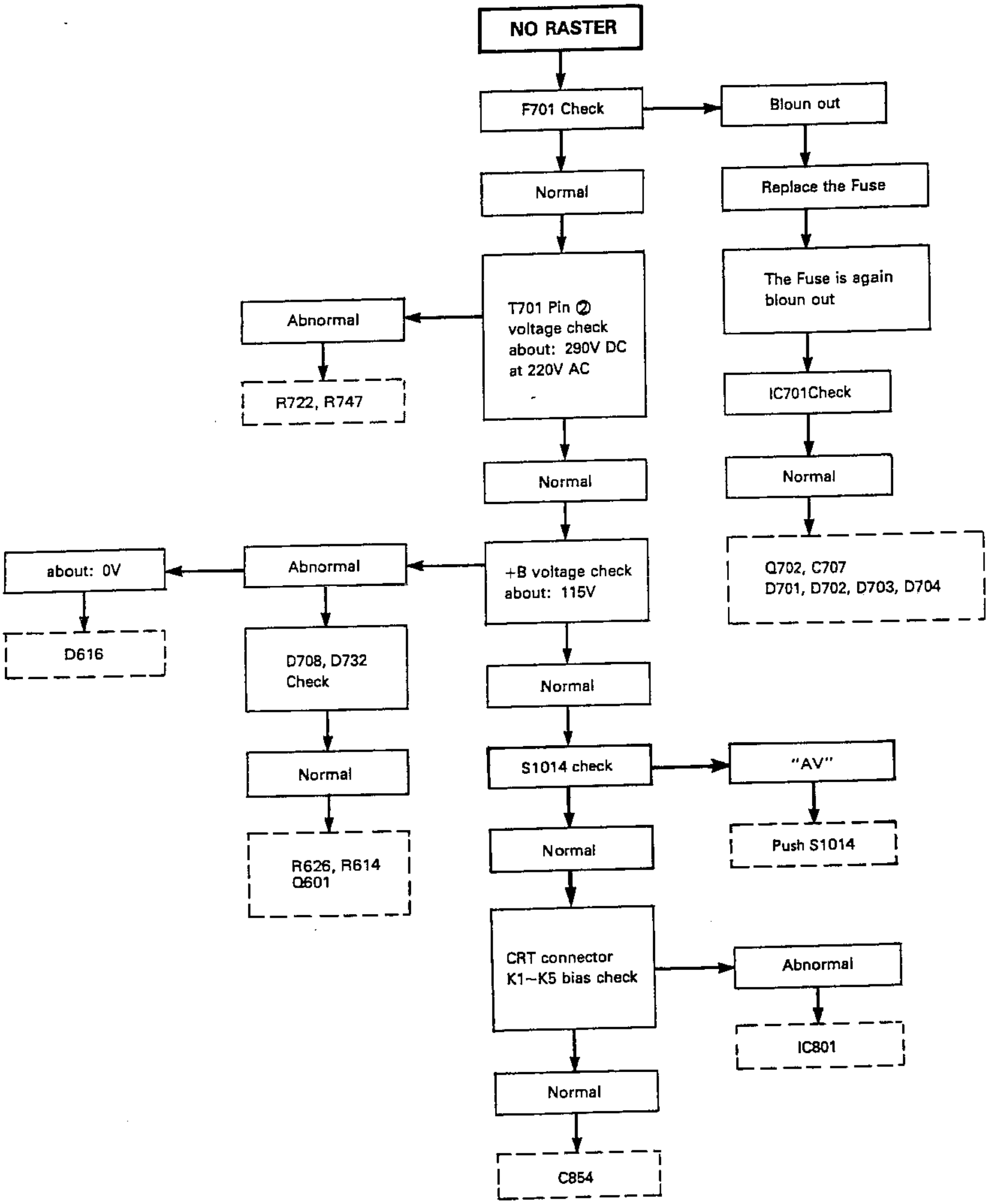
CRT DISPLAY ADJUSTMENT

Sign position control: R1022

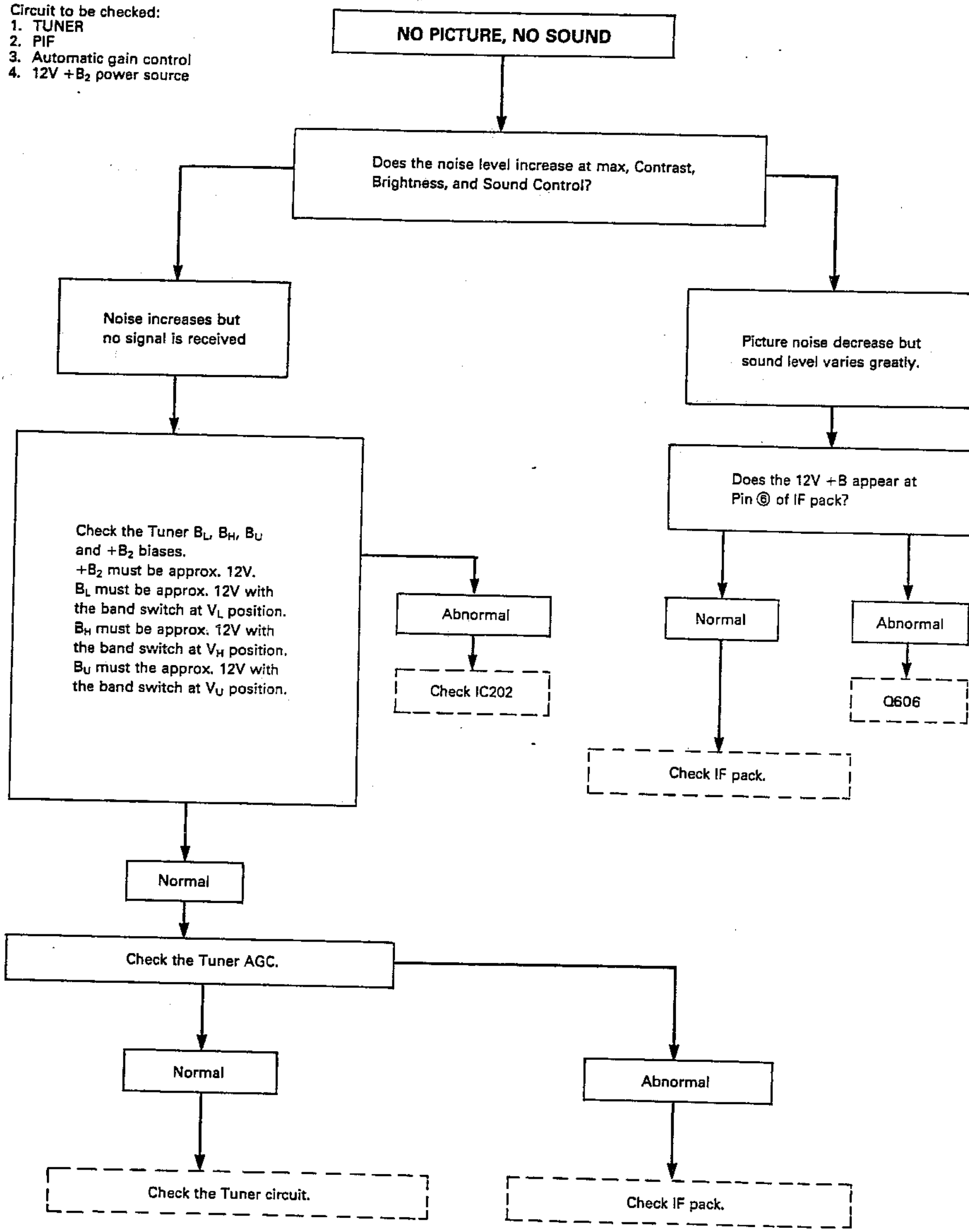
1. Set the channel at 2 ch.
2. Display the channel sign by means of the channel call of remote control on the screen. (Large Size)
3. Adjust the sign position by R1022 so that it is set 30 mm away from the CRT edge.



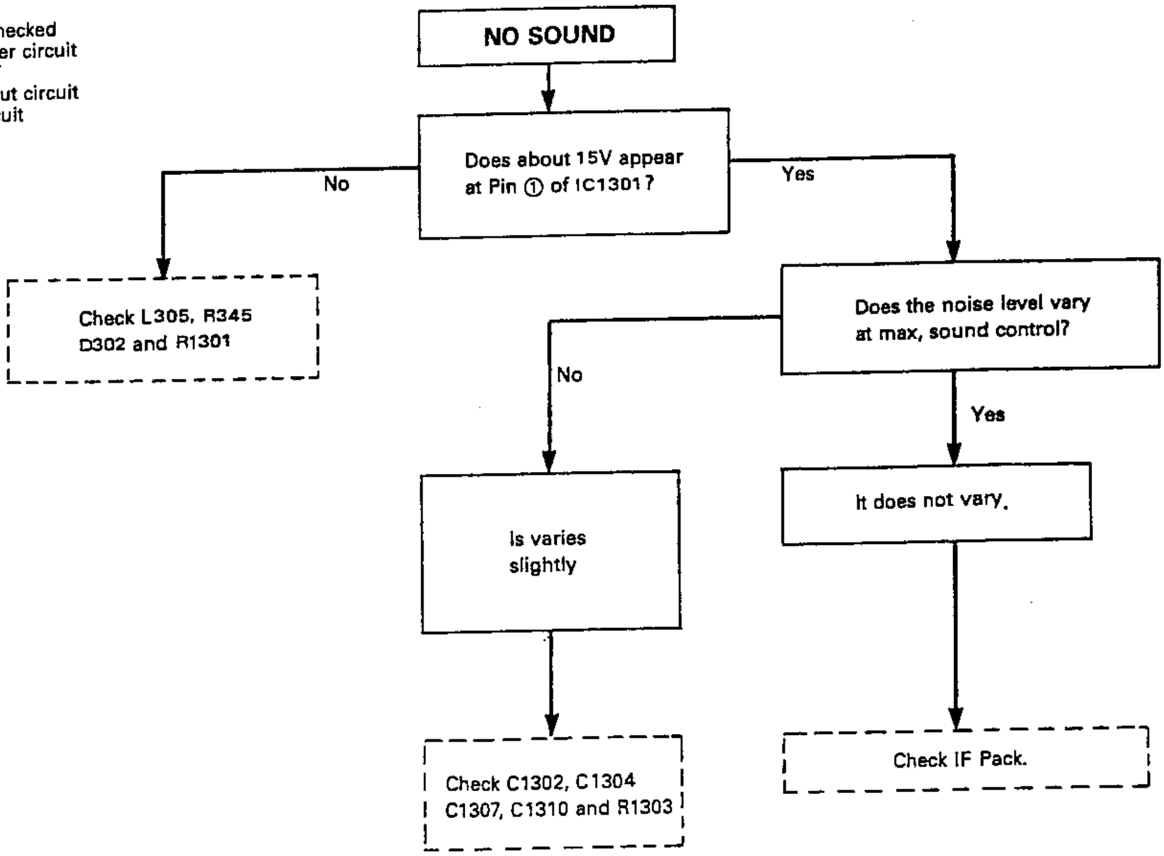
TROUBLE SHOOTING TABLE



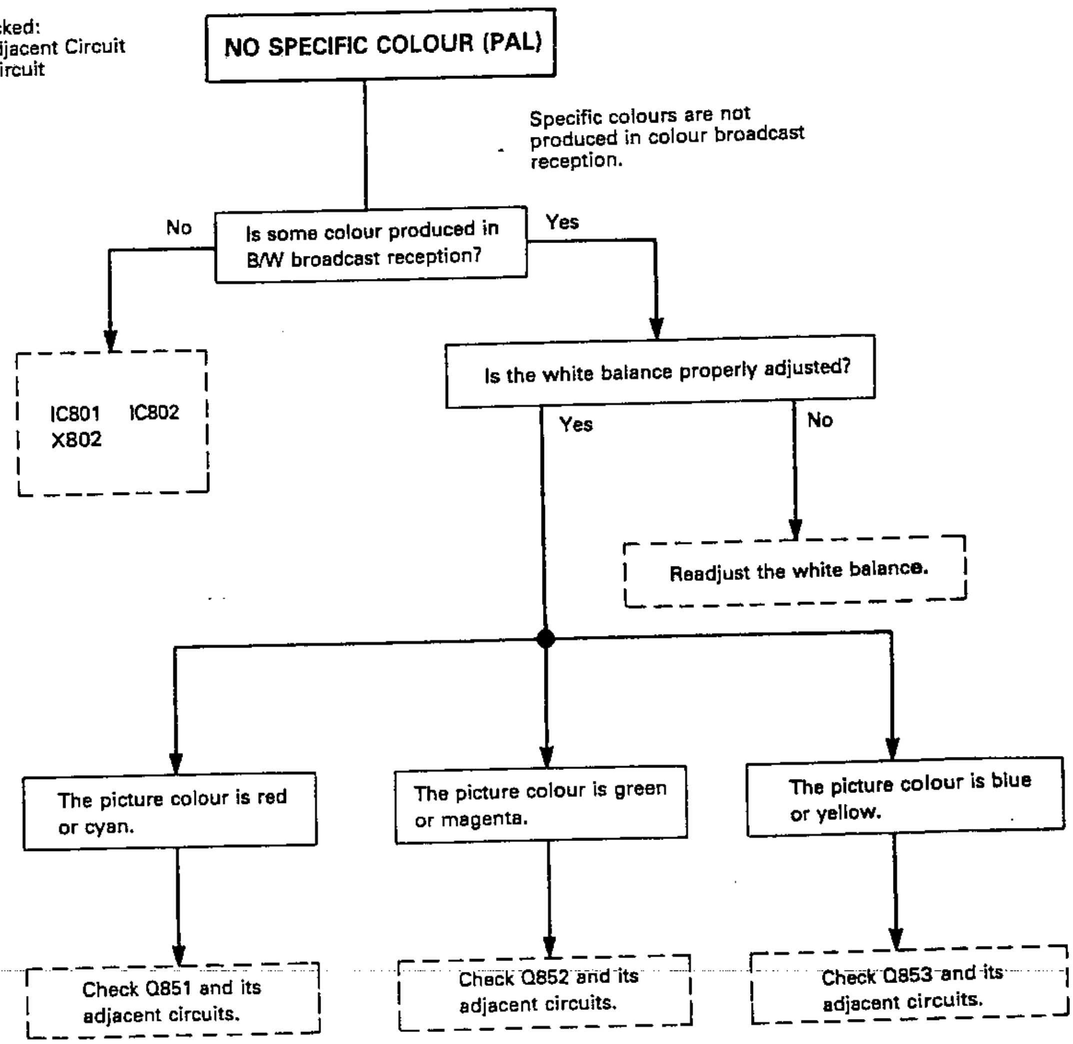
Circuit to be checked:
1. TUNER
2. PIF
3. Automatic gain control
4. 12V $+B_2$ power source



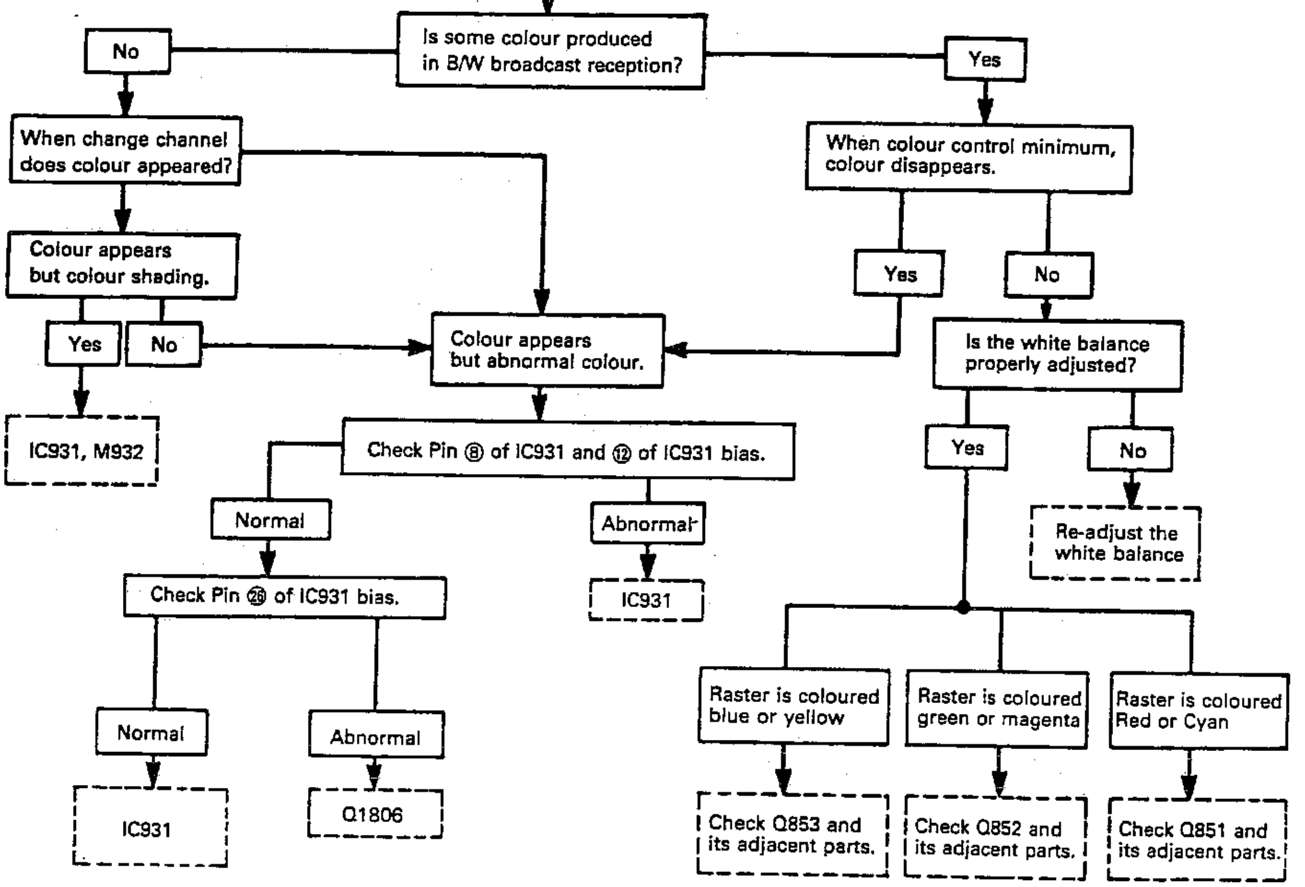
Circuit to be checked
1. SIF Amplifier circuit
2. Sound DET
3. Audio output circuit
4. Muting circuit



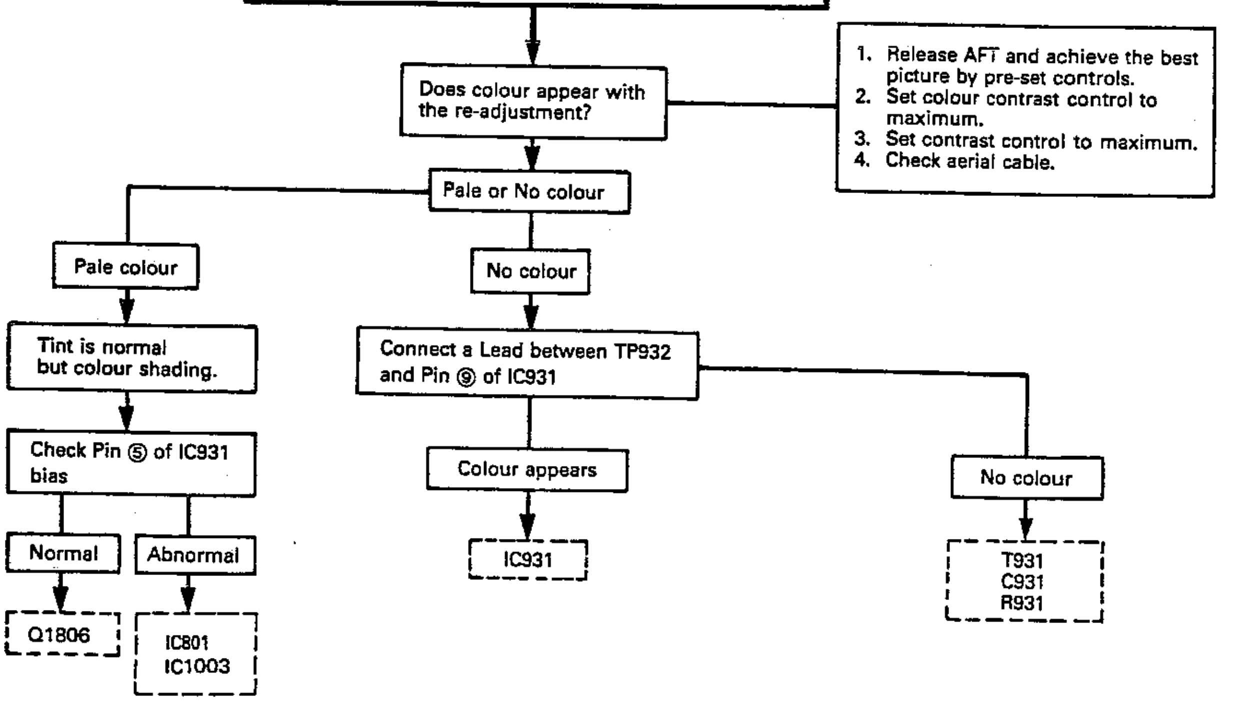
Circuits to be checked:
- IC801 and its Adjacent Circuit
- R.G.B. Output Circuit



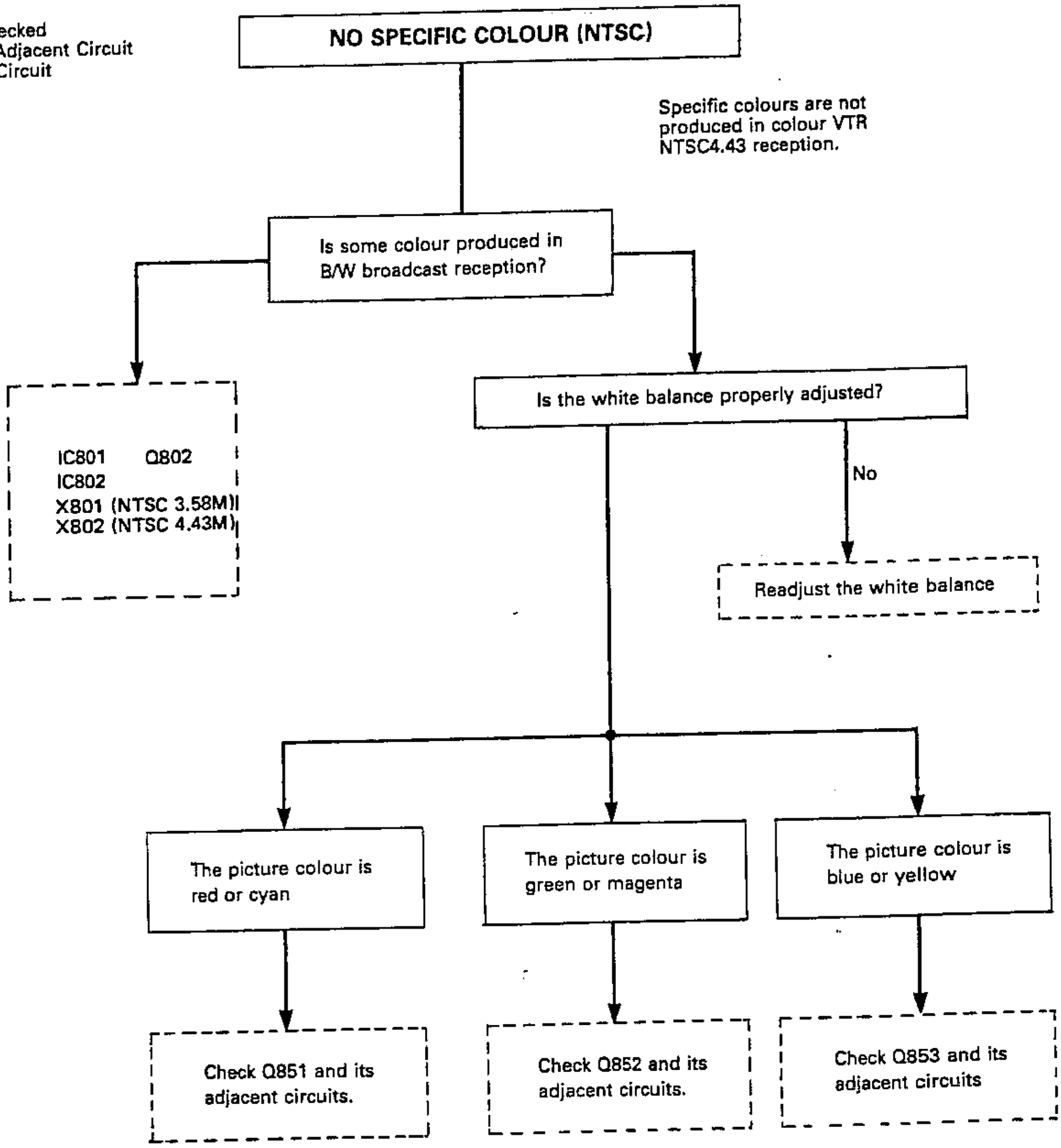
NO SPECIFIC COLOUR (SECAM)

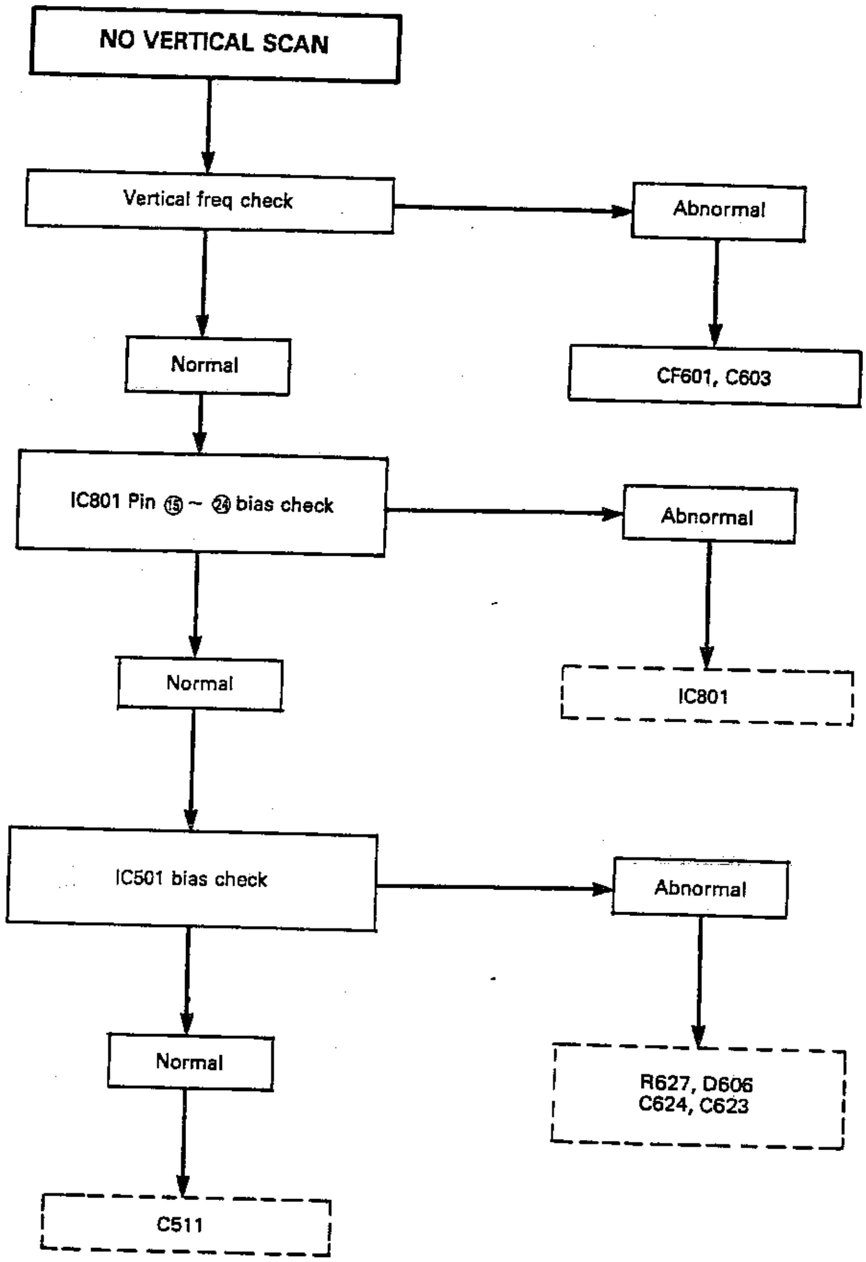


NO COLOUR OR PALE COLOUR (SECAM)

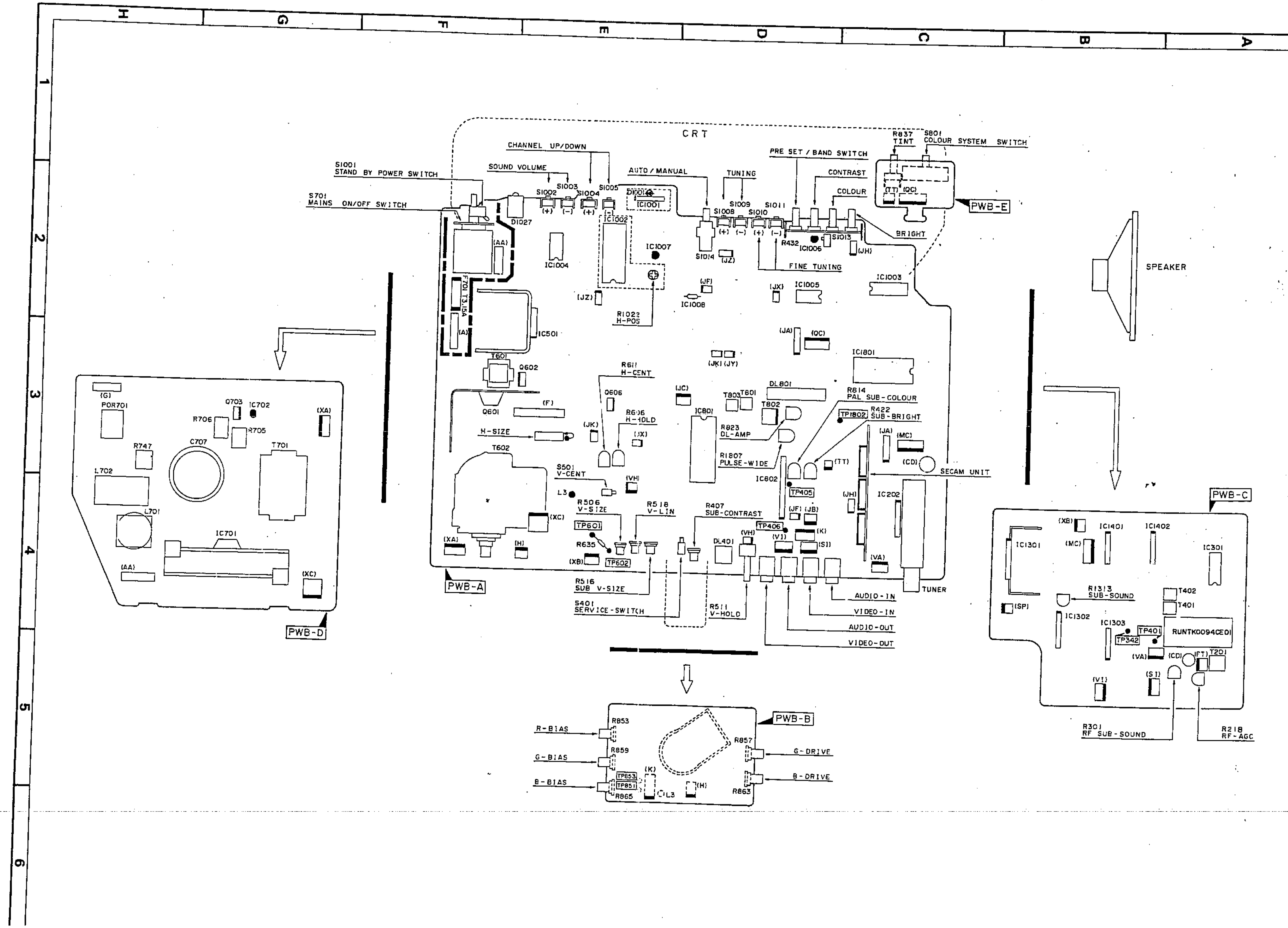


Circuits to be checked
- IC801 and its Adjacent Circuit
- R.G.B Output Circuit




NO VERTICAL SCAN
Vertical freq check
Abnormal
CF601, C603
Normal
IC801 Pin ⑮ ~ ㉔ bias check
Abnormal
IC801
Normal
IC501 bias check
Abnormal
R627, D606
C624, C623
Normal
C511

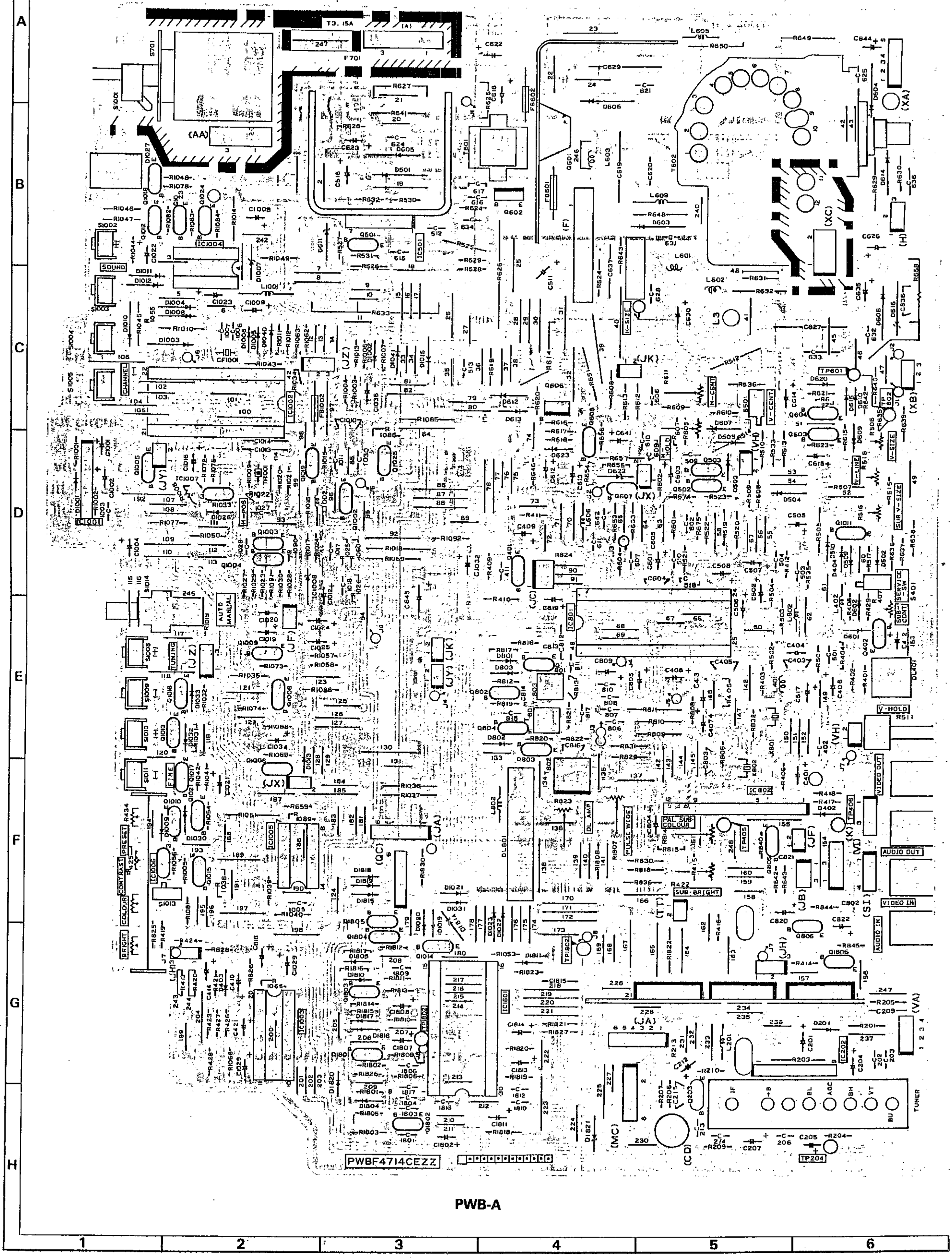
CHASSIS LAYOUT



DV-

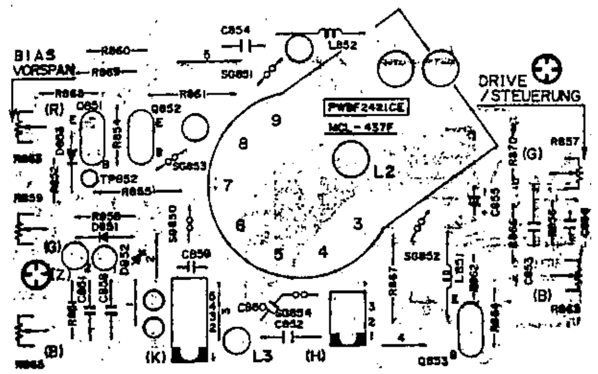
PRINTED WIRING BOARD ASSEMBLIES

(All the PWBs here are shown as viewed from their wiring sides.)

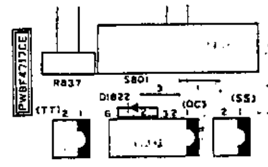


PWB-A

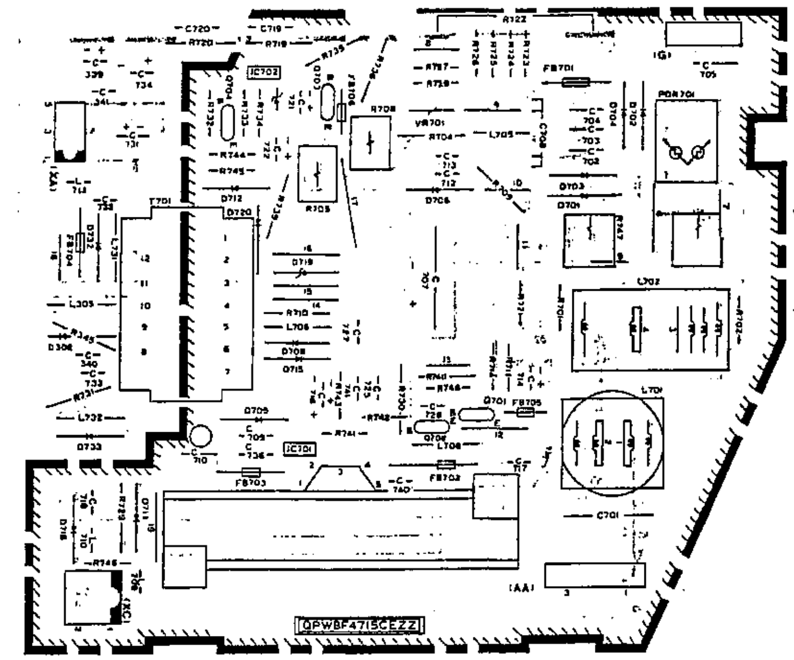
 DV-1410SPN



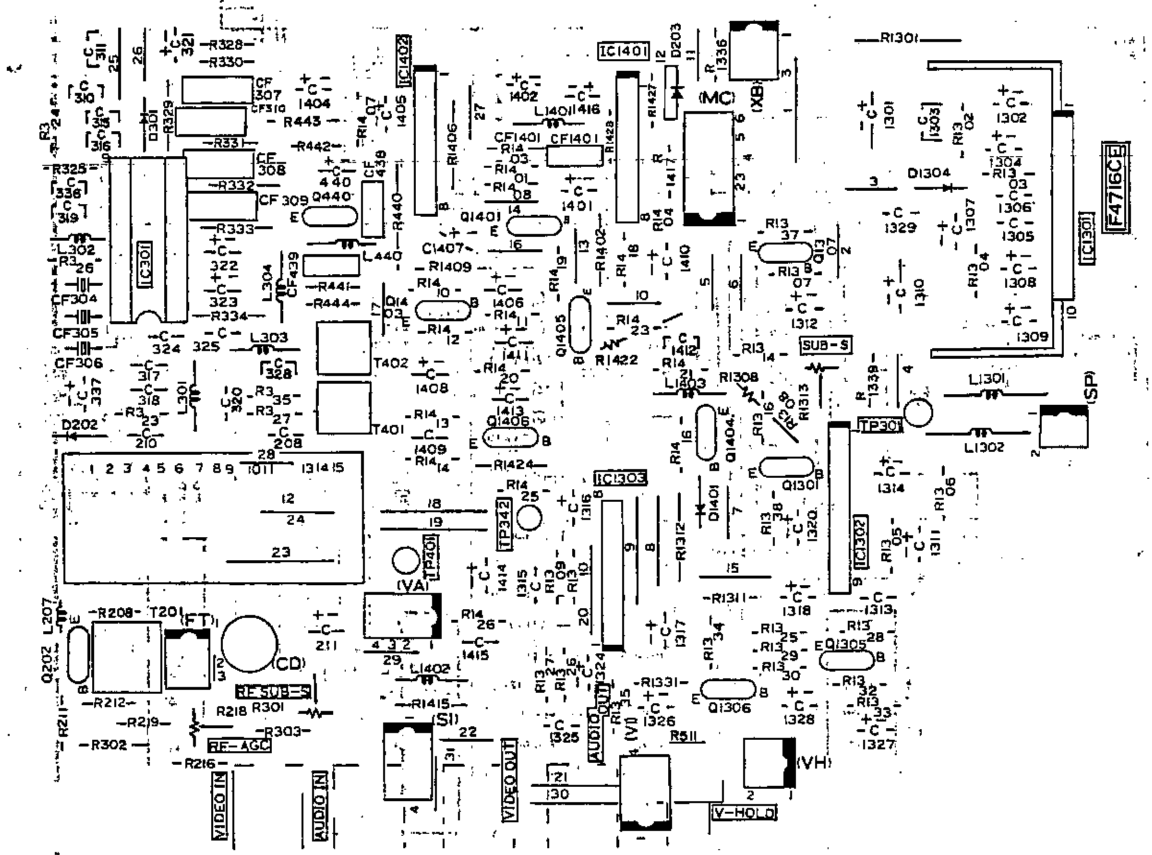
PWB-B



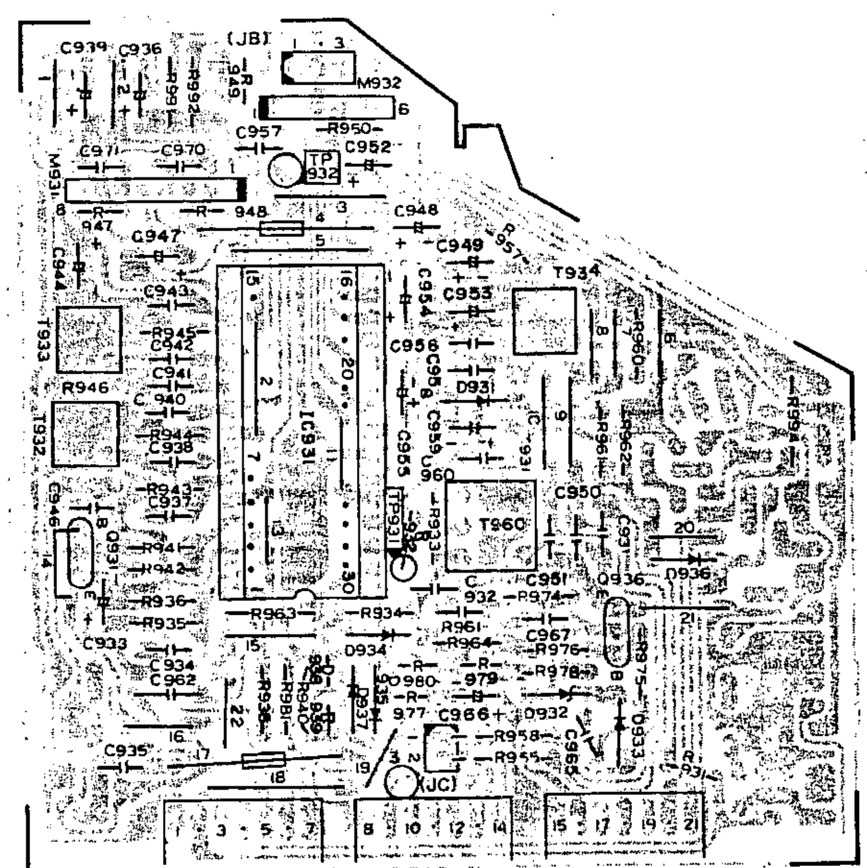
PWB-E



PWB-D

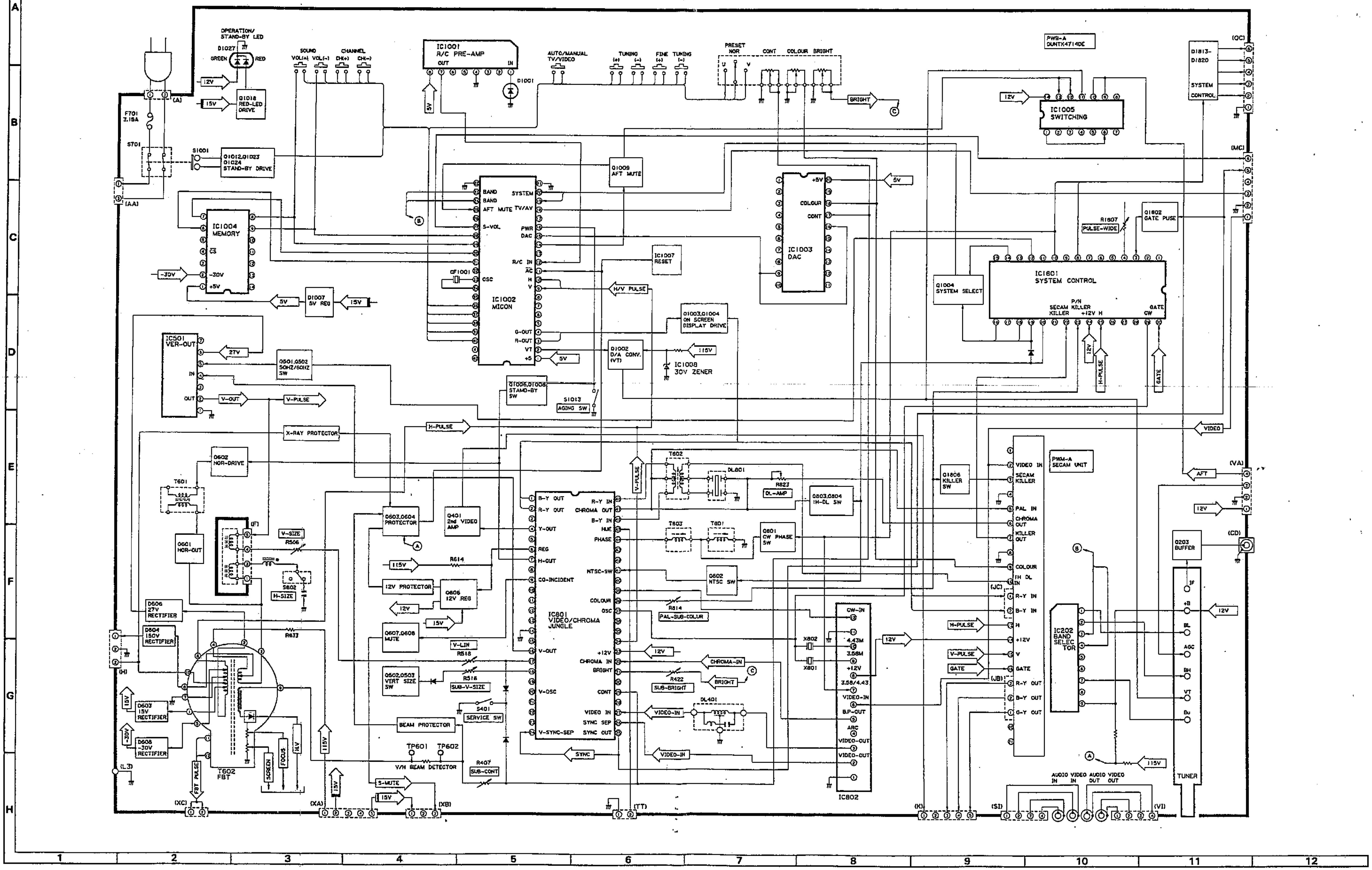


PWB-C

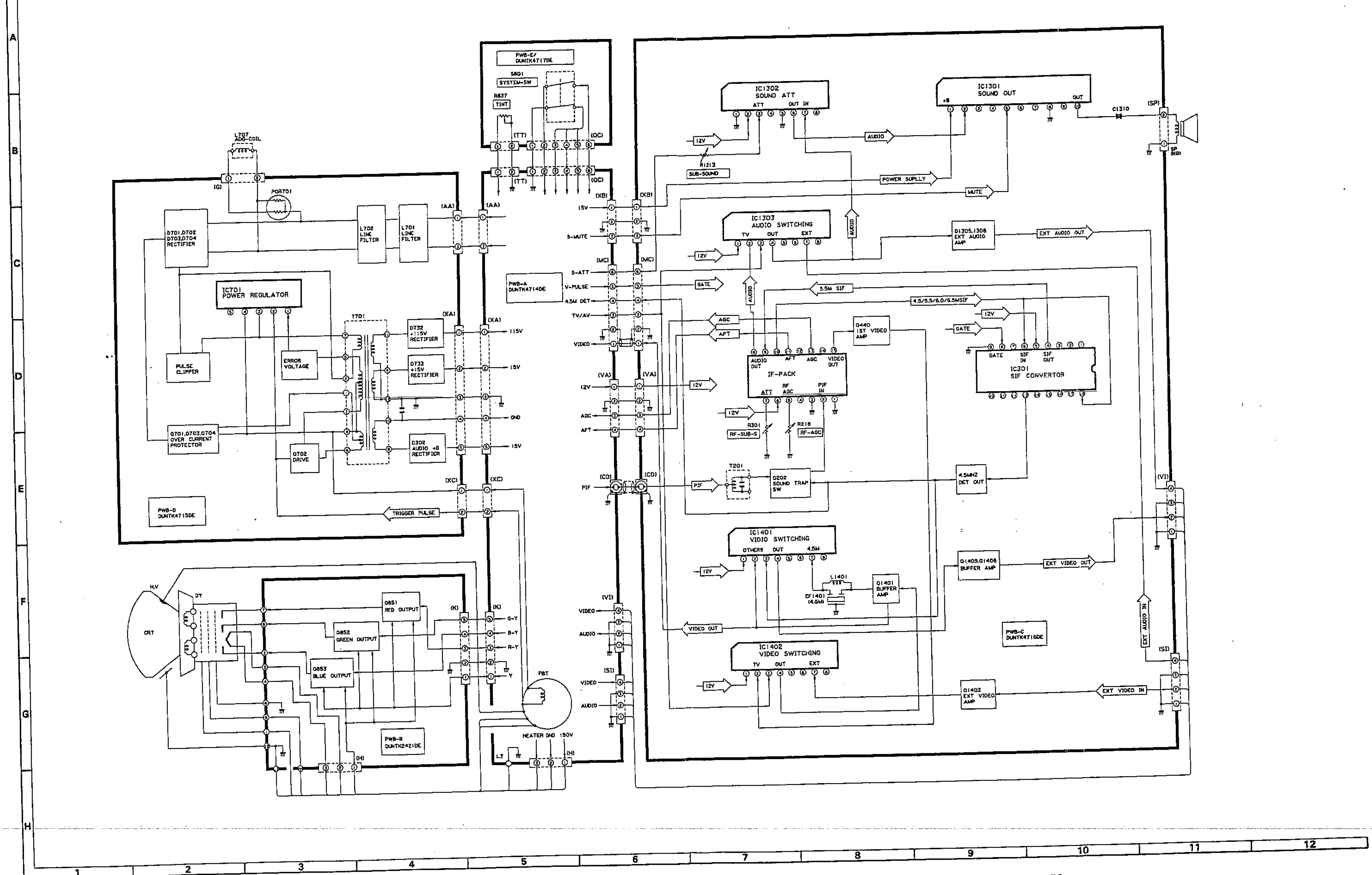


SECAM Unit

BLOCK DIAGRAM (MAIN)



BLOCK DIAGRAM (SUB)



SCHEMATIC DIAGRAMS AND WAVEFORMS

SERVICE PRECAUTION:

The area enclosed by this line (– – – –) is directly connected with AC Mains Voltage.
When servicing the area, connect an isolating transformer between TV receiver and AC line to eliminate hazard of electric shock.
Always turn the main power switch off or unplug the AC cord when replacing parts. Even with the POWER OFF this television unit will be in stand-by, that is, some of the electrical circuits will still be functioning with +B voltage (approximately 120 volts).

PARTS MARKED WITH "⚠" (   ) ARE IMPORTANT FOR MAINTAINING THE SAFETY OF THE SET. BE SURE TO REPLACE THESE PARTS WITH SPECIFIED ONES FOR MAINTAINING THE SAFETY AND PERFORMANCE OF THE SET.

CAUTION:
This circuit diagram is original one, therefore there may be a slight difference from yours.

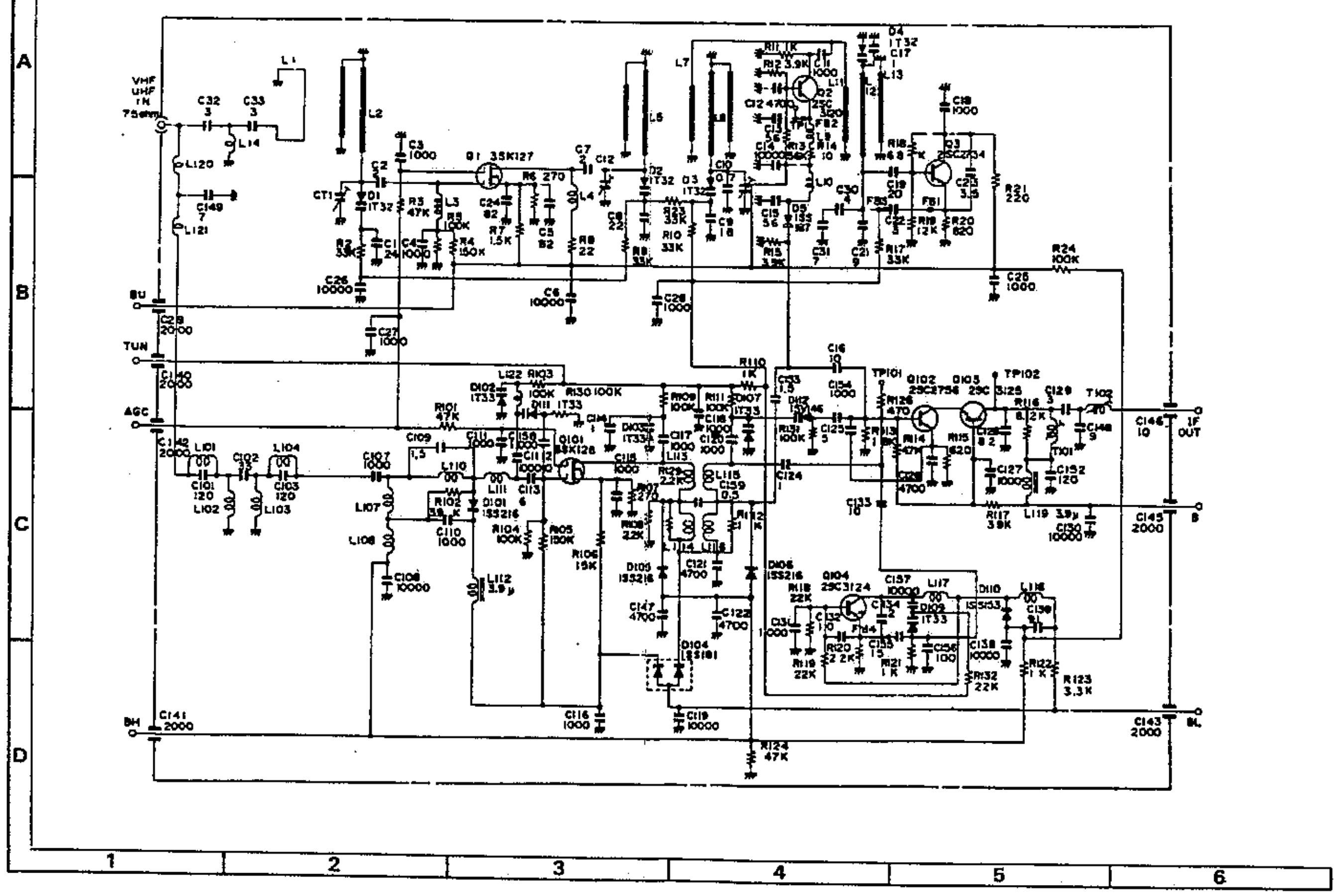
NOTES:

Voltage Measurement Conditions
1. *The voltage without parenthesis represents the value measured with PAL colour signal.*
2. *The voltage in parenthesis represents the value measured with SECAM colour signal.*
3. *All the voltages were measured by using a high impedance voltmeter.*

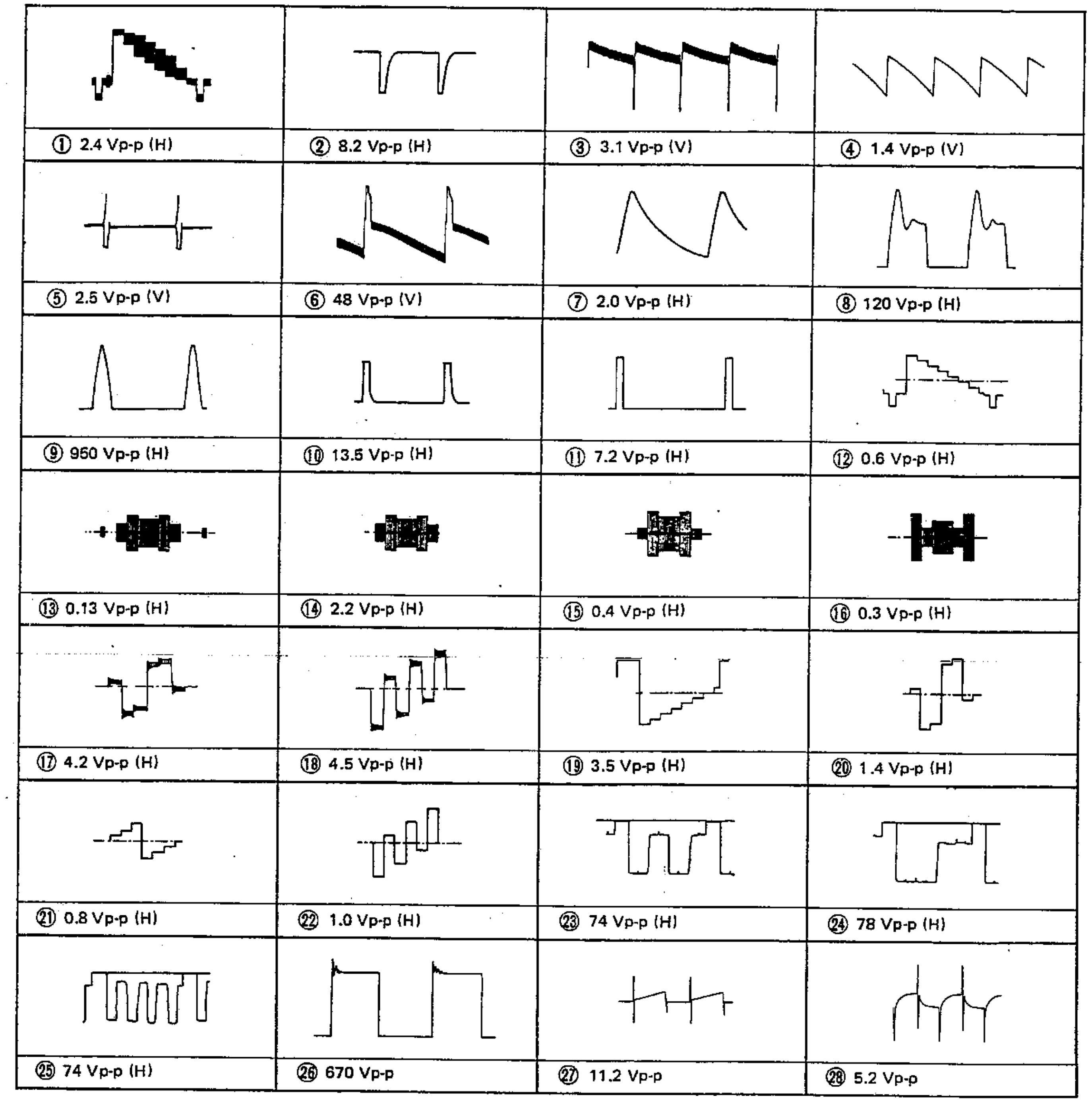
Waveform Measurement Conditions
1. *The colour bar signal applied to the base of Q202 is 2 V peak-to-peak.*
2. *The tuner AGC voltage is approximately 4 V.*

The diodes, whose parts code is not described, are the DX0179CE.

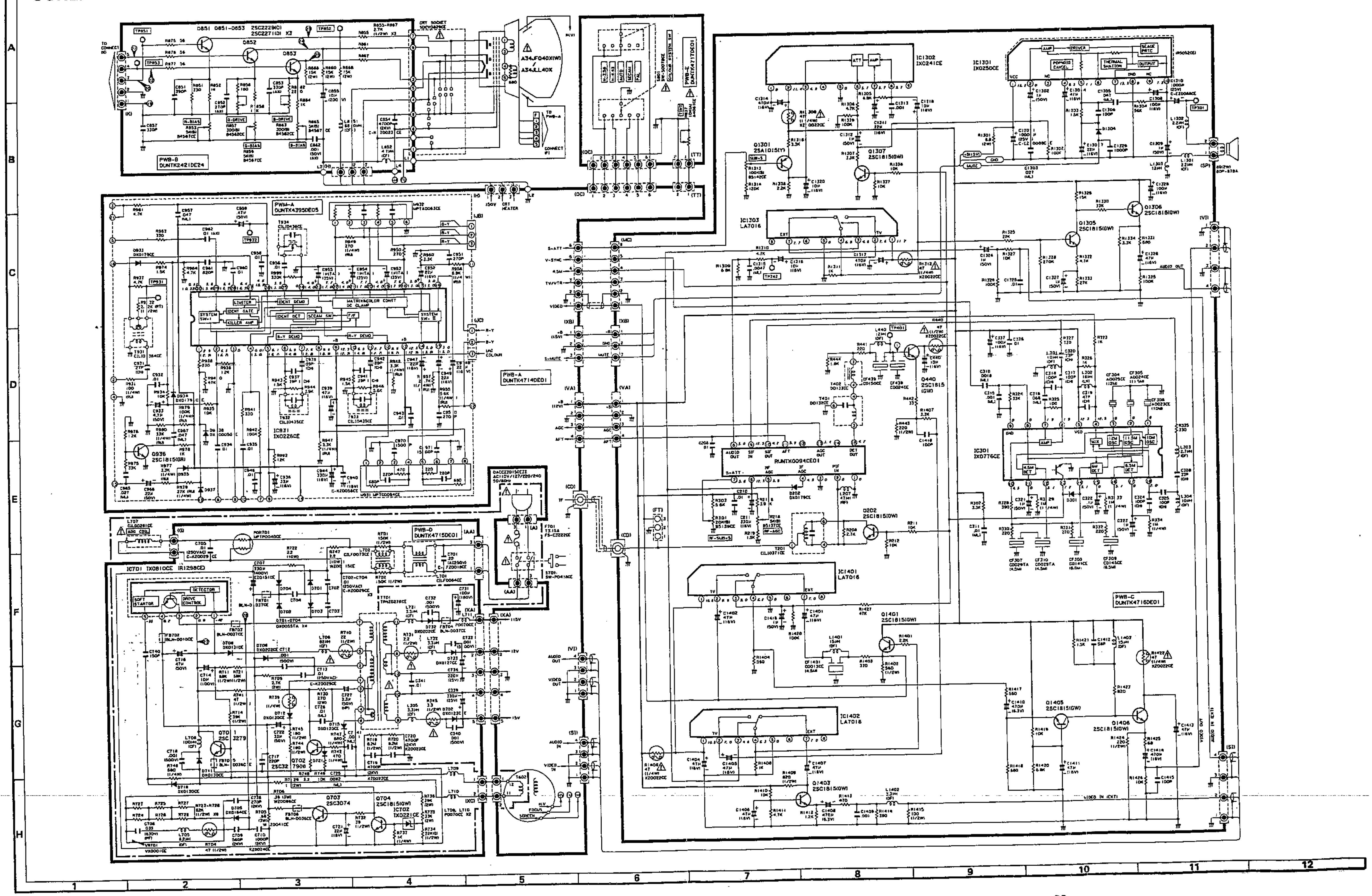
TUNER ⚠VTUVTS-1S1H//

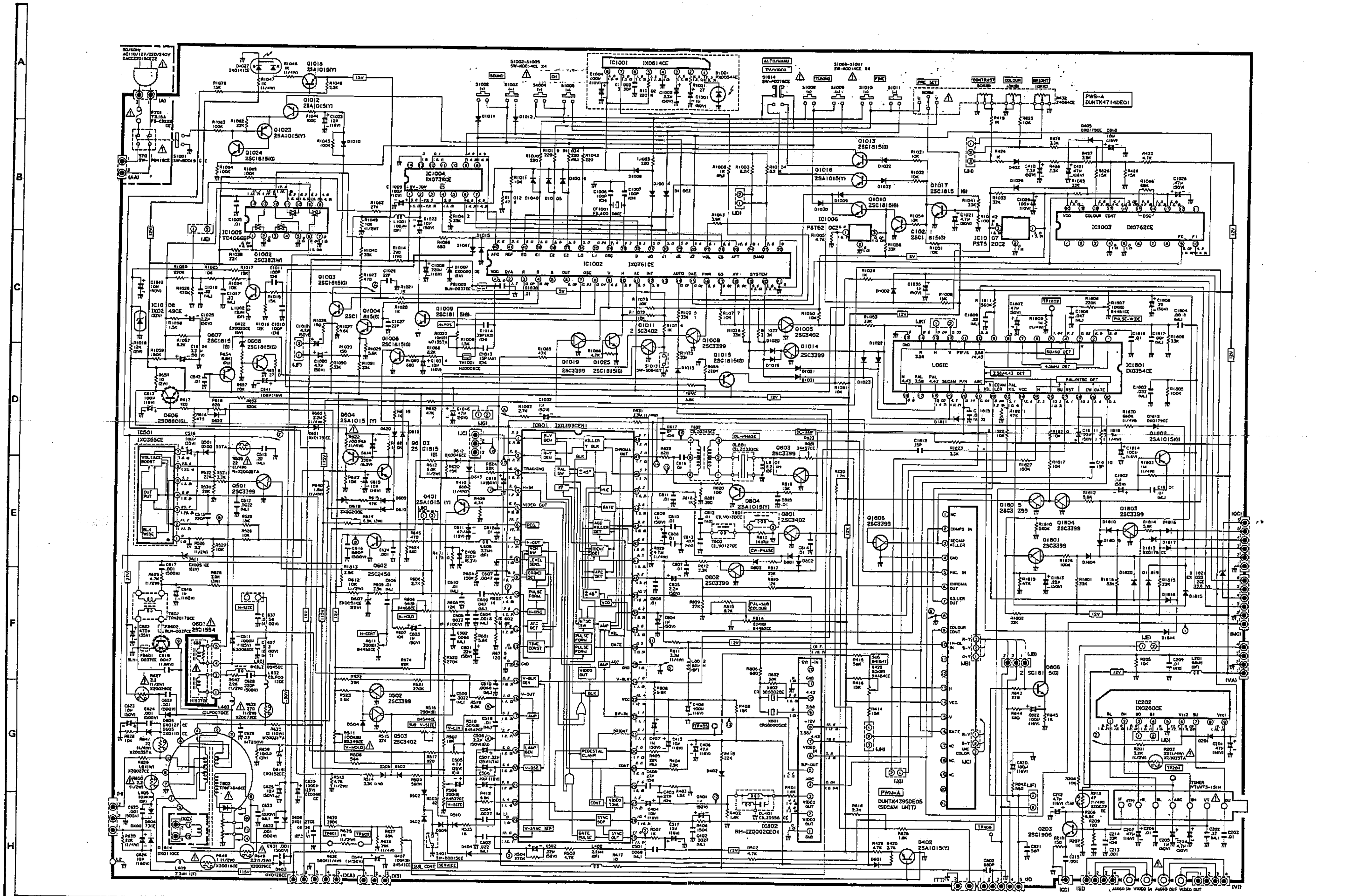


WAVE FORMS

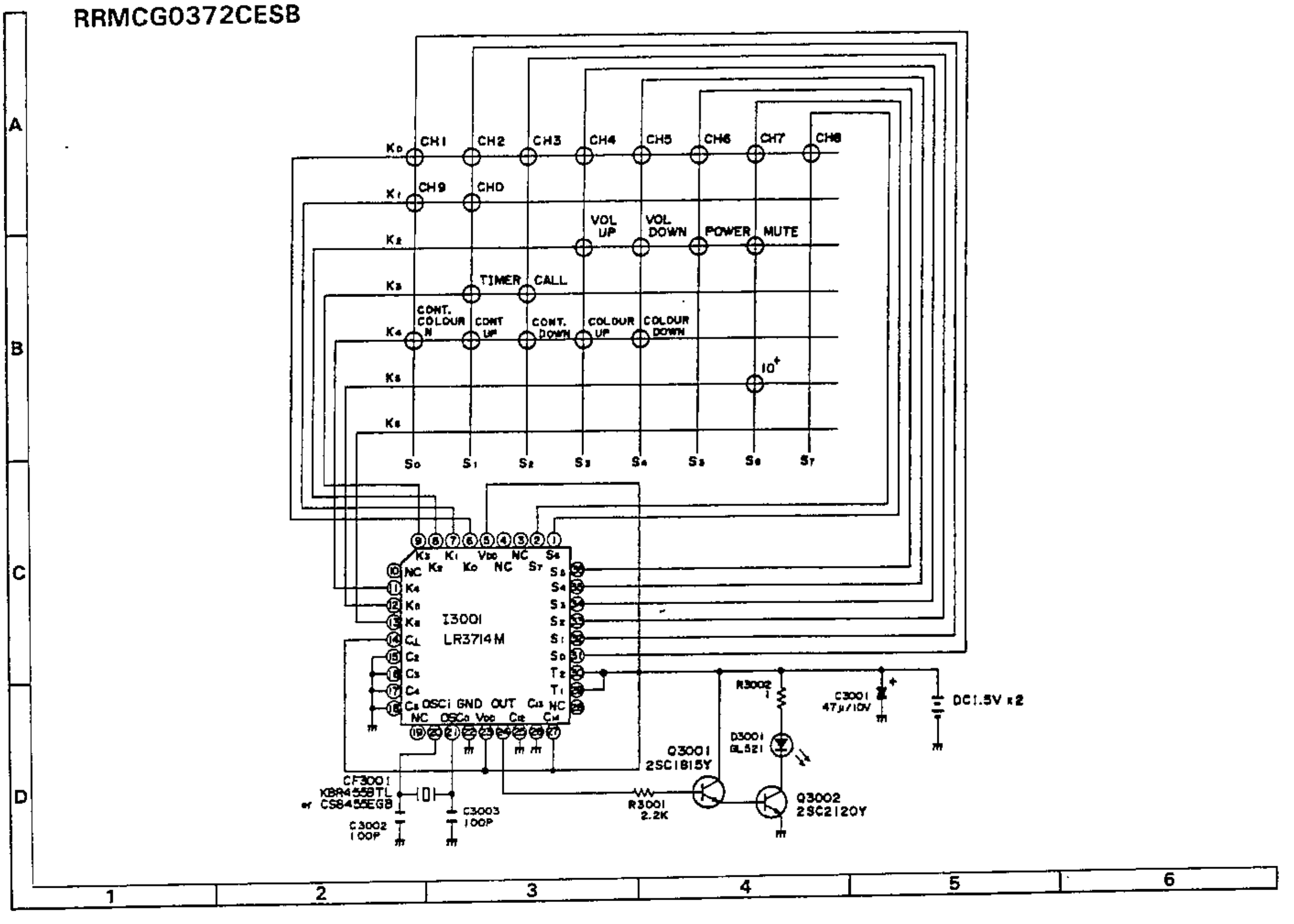


SCHEMATIC DIAGRAM





REMOTE CONTROL TRANSMITTER
RRMCG0372CESB



PARTS LIST

PARTS REPLACEMENT

Replacement parts which have these special safety characteristics identified in this manual; electrical components having such features are identified by ⚠ in the Replacement Parts Lists.
The use of a substitute replacement part which does not have the same safety characteristics as the factory recommended replacement parts shown in this service manual may create shock, fire or other hazards.

"HOW TO ORDER REPLACEMENT PARTS"

To have your order filled promptly and correctly, please furnish the following informations.

1. MODEL NUMBER 2. REF. NO.
3. PART NO. 4. DESCRIPTION

Ref. No.	Part No.	Description	Code
PICTURE TUBE			
⚠	VB34JFQ40X/ *S	CRT Ass'y	CF
	or		
⚠	VB34JLL40X/ *J		CF
⚠L707	RCiLG0261CEZZ	Degaussing Coil	AL
⚠	RCiLH1537CEN5	Deflection Yoke	BA
	or		
⚠	RCiLH1537CEZZ		BA
PRINTED WIRING BOARD ASSEMBLIES (NOT REPLACEMENT ITEM)			
PWB-A	DUNTK4714DE01	Mother Unit	–
PWB-B	DUNTK2421DE24	CRT Socket Unit	–
PWB-C	DUNTK4716DE01	AV/PIF Unit	–
PWB-D	DUNTK4715DE01	Power Unit	–
PWB-E	DUNTK4717DE01	System/Mode Switch	–
PWM-A	DUNTK4395DE05	SECAM Unit	–
PWB-A DUNTK4714DE01			
TUNER AND ASSEMBLY UNITS			
NOTE: THE PARTS HERE SHOWN ARE SUPPLIED AS AN ASSEMBLY BUT NOT DEPENDENTLY			
⚠	VTUVTS-1S1H//	VHF/UHF Tuner	BH
INTEGRATED CIRCUITS			
IC202	RH-iX0260CEZZ		AF
IC501	RH-iX0355CEZZ		AS
IC801	RH-iX0393CEN1		AW
IC802	RH-iZ0002CE01		AK
IC1001	RH-iX0614CEZZ		AH
IC1002	RH-iX0761CEZZ		AZ
IC1003	RH-iX0762CEZZ		AN

Ref. No.	Part No.	Description	Code
IC1004	RH-iX0738CEZZ		AU
IC1005	VHiTC4066BP-1		AL
IC1006, 1007	VHiPST520C2-1		AT
IC1008	RH-iX0249CEZZ		AE
IC1801	RH-iX0354CEZZ		AR
TRANSISTORS			
Q203	VS2SC1906//1E	2SC1906	AC
Q401, 402, 804, 1012, 1016, 1018, 1023	VS2SA1015Y/1E	2SC1015(Y)	AC
Q501, 502, 802, 803, 805, 1014, 1019, 1801, 1803 | 1806	VS2SC3399//-1	2SC3399	AB
Q503, 801, 1005, 1011	VS2SC3402//-1	2SC3402	AB
⚠Q601	VS2SD1554//1E	2SD1554	AL
Q602	VS2SC2456//1E	2SC2456	AE
⚠Q603, 607, 608, 806, 1004, 1006, 1009, 1010, 1013, 1015, 1017, 1021, 1024, 1025	VS2SC1815GW-1	2SC1815(GW)	AB
⚠Q604 1802	VS2SA1015GW-1	2SA1015(GW)	AC
Q606	VS2SD880GLB-1	2SD880	AF
Q1002	VS2SC383-WT-1	2SC383	AE
DIODES			
D201, 402, 403, 404, 502 | 505, 509, 510, 601,	RH-DX0179CEZZ	1SS177	AA

Ref. No.	Part No.	Description	Code
602, △609, △610, 613, △615, △620, △621, 623, 801, 802, 803, 1002–1006, 1008–1013, 1015, 1019–1023, 1026, 1030–1033, 1040, 1041, 1804, 1805, 1810–1820			
D501	RH-DX0055TAZZ	1S1888	AD
D603	RH-DX0126CEZZ		AC
D604	RH-DX0073CEZZ	ERB24-02B	AD
D605, 614	RH-DX0110CEZZ	S5277G	AB
D606, 608	RH-DX0127CEZZ	1S5295G	AC
D607, 611	RH-EX0051CEZZ	RD22E Zener Diode	AB
D612	RH-DX0046CEZZ	1S2471	AC
D616	RH-EX0152CEZZ	Zener Diode	AE
D619, 622, 1007	RH-EX0020GEZZ	RD5.1EB3 Zener Diode	AE
D1001	RH-PX0004AEZZ	Photo Diode	AK
D1027	RH-PX0141CEZZ	LED	AE
D1821	RH-EX0232CEZZ	Zener Diode	AB
TH1001	RH-HZ0006CEZZ	Thermistor	AB

PACKAGED CIRCUITS

Ref. No.	Part No.	Description	Code
X801	RCRSB0005CEZZ	Crystal	AN
X802	RCRSB0002CEZZ	Crystal	AM

COILS

Ref. No.	Part No.	Description	Code
L201, 802	VP-DF680K0000	68μH	AB
L402	VP-DF2R2K0000	2.2μH	AB
L601	RCiLZ0545CEZZ		AF
L602	RCiLP0013GEZZ		AD
L603	RCiLP0070CEZZ		AD
L605	VP-DF100K0000	10μH	AB
L606	VP-DF3R3K0000	3.3μH	AB
L609	VP-CF3R3K0000	3.3μH	AB
L801	VP-DF8R2K0000	8.2μH	AB
L1001	VP-DF101K0000	100μH	AB
L1002	VP-DF120K0000	12μH	AB

CERAMIC FILTERS

Ref. No.	Part No.	Description	Code
CF1001	RFiLA0008CEZZ		AE

DELAY LINES

Ref. No.	Part No.	Description	Code
DL401	RCiLZ0556CEZZ		AG
DL801	RCiLZ0333CEZZ		AR

TRANSFORMERS

Ref. No.	Part No.	Description	Code
T601	RTRNZ0179CEZZ		AE
△T602	RTRNF1646CEZZ		BG
T801	RCiLV0130CEZZ		AD
T802	RCiLZ0345CEZZ		AD
T803	RCiLV0127CEZZ		AD

CONTROLS

Ref. No.	Part No.	Description	Code
R407	RVR-B4543CEZZ	100k(B) Sub-Contrast	AB
R422	RVR-B4464CEZZ	50k(B) Sub-Brightness	AC
△R432	RVR-Z4064CEZZ	Pre-Set/User Controls	AH
R506	RVR-B4532CEZZ	200(B) Vertical Size	AB
△R511	RVR-B5349CEZZ	100k(B) Vertical Hold	AC
R516	RVR-B4544CEZZ	200k(B) Sub-Vertical Size	AB
R518	RVR-B4542CEZZ	50k(B) Vertical Line	AB
R606	RVR-B4460CEZZ	5k(B) Horizontal Hold	AC
R611	RVR-B4455CEZZ	300(B) Horizontal Cent	AC
R814	RVR-B4462CEZZ	20k(B) PAL-Sub-Colour	AC
R823	RVR-B4457CEZZ	1k(B) DL Amp.	AC
R1022	RVR-M7135TAZZ	10k(B) Horizontal Position	AC
R1807	RVR-B4461CEZZ	10k(B) Pulse-Wide	AC

CAPACITORS

Ref. No.	Part No.	Description	Code
C408, 613, 641, 820, 822, 1814	VCEAAA1CW107M	100 16V Electrolytic	AB
C409	VCEAAA0JW227M	220 6.3V Electrolytic	AB
C507	VCSATA1VE334K	0.33 35V Tantalum (N.P.)	AC
C511, 630	RC-EZ0088CEZZ	1000 25V Electrolytic	AE
C516	VCEAAA1VW107M	100 35V Electrolytic	AC
C605	VCQPSA2AA332J	3300p 100V	AC
△C614	VCEAGA0JW337M	330 6.3V Electrolytic	AB
△C615	VCEAAA1CW106M	10 16V Electrolytic	AB
C616	VCKYPA2HB681K	680p 500V Ceramic	AA

Ref. No.	Part No.	Description	Code
C617, 621, 624, 625, 631, 632	VCKYPA2HB102K	1000p 500V Ceramic	AA
C618	VCEAAA2CW105M	1 160V Electrolytic	AB
C619	VCFPPD3CA472J	4700p 1.6kV Metalized Polypro Film	AD
C622	VCEAAA1VW107M	470 35V Electrolytic	AD
C626	VCEAAA2CW106M	10 160V Electrolytic	AC
C627	VCFPPD2DB334J	0.33 200V Metalized Polypro Film	AF
C628	VCKYPA2HB221K	220p 500V Ceramic	AA
C629	VCFPPD2DB224J	0.22 200V Metalized Polypro Film	AE
C633	VCQYSH2DM104K	0.1 200V Mylar	AD
C636	VCFYSB2EB104K	0.1 250V	AC
C637	VCFYSB2GB563K	0.056 400V	AD
C1004, 1009, 1029	VCEAAA1AW107M	100 10V Electrolytic	AB
C1008	VCEAGA1AW227M	220 10V Electrolytic	AB
RESISTORS			
△R203, △ 525, △ 641	RR-XZ0035TAZZ	22 1/4W Fuse Resistor	AB
△R213	RR-XZ0022CEZZ	47 1/4W Fuse Resistor	AB
R514	VRS-VV3AB332J	3.3k 1W Metal Oxide	AA
R614	VRS-VV3LB682J	6.8k 3W Metal Oxide	AB
△R615, △ 642	VRD-RA2BE473J	47k 1/8W Carbon	AA
△R619	VRD-RA2BE102J	1k 1/8W Carbon	AA
△R621, △ 623	VRD-RA2BE103J	10k 1/8W Carbon	AA
△R622	VRD-RU2EE101J	100 1/4W Carbon	AA
R626	VRS-PV3LB392J	3.9k 3W Metal Oxide	AB
△R627 △ 649	RR-XZ0029CEZZ	3.3 1/2W Fuse Resistor	AB
R629	VRN-RV3AB1R5J	1.5 1W Metal Film	AA
△R632	RR-XZ0073CEZZ	270 1/2W Fuse Resistor	AB
R633	RR-WZ0031TAZZ	12 10W Cement	AE
R635	VRS-PU2HB102J	1k 1/2W Metal Oxide	AA
△R648	RR-XZ0016CEZZ	1 1/2W Fuse Resistor	AB
△R650	RR-XZ0027CEZZ	2.2 1/2W Fuse Resistor	AB
R651	VRS-VV3DB100J	10 2W Metal Oxide	AA
R658	VRS-VV3LB103J	10k 3W Metal Oxide	AB
R1014	VRS-VV3AB391J	390 1W Metal Oxide	AA
R1018	VRS-VV3DB123J	12k 2W Metal Oxide	AA
SWITCHES			
S401	QSW-B0015CEZZ	Servise	AC
△S701	QSW-P0418CEZZ	Main Switch	AK
△S1001	QSW-B0019CEZZ	Sub Power Switch	AF
△S1002, △ 1003, △ 1004, △ 1005, △ 1008, △ 1009, △ 1010, △ 1011	QSW-K0014CEZZ	Sound (+), Sound (−), Channel (+), Channel (−), Tuning (+), Tuning (−), Fine (+), Fine (−)	AC

Ref. No.	Part No.	Description	Code
S1013	QSW-S0048TAZZ	Aging Switch	AD
△S1014	QSW-P0378CEZZ	TV/AV Switch	AE
MISCELLANEOUS			
△F701	QFS-C3222CEZZ	Fuse-T3.15A	AE
△	QFSHD1002CEZZ	Fuse Holder	AA
△	QJAKE0016GEZZ	Jack, Audio In/Out	AC
△	QJAKE0017GEZZ	Jack, Video In/Out	AC
FB601, 602, 1002	RBLN-0037CEZZ	Ferrite Bead	AB

PWB-B DUNTK2421DE24

Ref. No.	Part No.	Description	Code
TRANSISTORS			
Q851 | 853	VS2SC2229ō/1E	2SC2229(ō)	AD
COIL			
L851	VP-CF681K0000	680μH	AB
CONTROLS			
R853, 859, 865	RVR-B4567CEZZ	5k(B) Red Bias, Green Bias, Blue Bias	AC
R857, 863	RVR-B4562CEZZ	300(B) Green Drive, Blue Drive	AC
CAPACITORS			
C854	RC-KZ0023CEZZ	4700p 2kV Ceramic	AD
C855	VCEAAA2DW106M	10 200V Electrolytic	AC
RESISTORS			
R855, 861, 867	VRC-MA2HG272K	2.7k 1/2W Solid	AA
R860, 866, 868	VRS-VV3DB153J	15k 2W Metal Oxide	AA
MISCELLANEOUS			
△	VSōCV0829CEZZ	CRT Socket	AK

PWB-C DUNTK4716DE01

Ref. No.	Part No.	Description	Code
INTEGRATED CIRCUITS			
IC301	RH-iX0776CEZZ		AN
IC1301	RH-iX0250CEZZ		AK

Ref. No.	Part No.	Description	Code
IC1302	RH-iX0241CEZZ		AF
IC1303, 1401, 1402	VHiLA7016/ /-1		AH
TRANSISTORS			
Q202, 440, 1305, 1306, 1307, 1401, 1403, 1405, 1406	VS2SC1815GW-1	2SC1815(GW)	AB
Q1301	VS2SA1015Y/1E	2SA1015(Y)	AC
DIODES			
D202, 301, 1304	RH-DX0179CEZZ	1SS177	AA
COILS			
L207	VP-RF470K0000	47μH	AB
L301, 304	VP-DF100K0000	10μH	AB
L302	VP-LK180K0000	18μH	AB
L303	VP-DF2R7K0000	2.7μH	AB
L440	VP-DF120K0000	12μH	AB
L1301, 1302	VP-CF2R2K0000	2.2μH	AB
L1303	VP-LK120K0000	12μH	AB
L1401, 1403	VP-DF150K0000	15μH	AB
L1402	VP-DF3R3K0000	3.3μH	AB
CERAMIC FILTERS			
CF304	RFiLA0025CEZZ	12M	AF
CF305	RFiLA0024CEZZ	11.5M	AF
CF306	RFiLA0023CEZZ	10M	AF
CF307, 310	RFiLC0029TAZZ	4.5M	AD
CF308	RFiLC0144CEZZ	6.0M	AD
CF309	RFiLC0145CEZZ	6.5M	AE
CF438	RFiLC0024CEZZ		AE
CF439	RFiLC0150CEZZ		AF
CF1401	RFiLC0013CEZZ	4.5M	AE
TRANSFORMERS			
T201	RCiLi0371CEZZ		AD
T401	RCiLD0132CEZZ		AD
T402	RCiLD0133CEZZ		AD
CONTROLS			
R218	RVR-B5137CEZZ	5k(B) RF-AGC	AB
R301	RVR-B5139CEZZ	20k(B) RF-Sub-Sound	AB
R1313	RVR-B5142CEZZ	100k(B) Sub Sound	AD
CAPACITORS			
C211	VCEAAA1CW337M	330 16V Electrolytic	AC
C337, 1308, 1328	VCEAAA1CW107M	100 16V Electrolytic	AB
C1301, 1310	RC-EZ0088CEZZ	1000 25V Electrolytic	AE
C1314, 1317, 1414	VCEAAA1CW477M	470 16V Electrolytic	AC
C1408, 1410	VCEAAA0JW477M	470 6.3V Electrolytic	AC
RESISTORS			
ΔR440, Δ 1308, Δ 1312, Δ 1406, Δ 1422	RR-XZ0022CEZZ	47 1/4W Fuse Resistor	AB
R1301	VRN-VV3DB6R8J	6.8 2W Metal Film	AB

PWB-D DUNTK4715DE01

Ref. No.	Part No.	Description	Code
INTEGRATED CIRCUITS			
ΔIC701	RH-iX0810CEZZ		AS
ΔIC702	RH-iX0221CEZZ		AE
TRANSISTORS			
ΔQ701	VS2SC3279/ /1E	2SC3279	AA
ΔQ702	VS2SC3279N/-1	2SC3279N	AC
ΔQ703	VS2SC3074/ /-1	2SC3074	AF
ΔQ704	VS2SC1815GW-1	2SC1815(GW)	AB
DIODES			
D302	RH-DX0123CEZZ	TVR1D	AC
ΔD701 | Δ 704	RH-DX0055TAZZ	1S1888	AD
ΔD705	RH-DX0164CEZZ	ES-1F	AC
ΔD706, 732	RH-DX0202CEZZ		AD
ΔD708	RH-DX0131CEZZ	EU-1	AC
ΔD711, Δ 712, Δ 715, Δ 718	RH-DX0130CEZZ	EU-1Z	AE
D721	RH-DX0179CEZZ	1SS177	AA
D733	RH-DX0127CEZZ	1S5295G	AC
ΔVR701	RH-VX0001CEZZ	Varistor	AF

Ref. No.	Part No.	Description	Code
PACKAGED CIRCUIT			
ΔPOR701	RMPTP0040CEZZ		AK
COILS			
L305, 731, 732	VP-CF3R3K0000	3.3μH	AB
ΔL701	RCiLF0064CEZZ		AG
ΔL702	RCiLF0073CEZZ		AG
ΔL705	VP-DF8R2K0000	8.2μH	AB
ΔL706	VP-CF820K0000	820μH	AB
ΔL708	VP-CF101K0000	100μH	AB
ΔL709, Δ 710, 711	RCiLP0070CEZZ		AD
TRANSFORMER			
ΔT701	RTRNZ0276CEZZ	REG.Transformer	AW
CAPACITORS			
C339	VCEAAA1EW337M	330 25V Electrolytic	AD
C340, Δ 712, Δ 718, 732, 733	VCKYPA2HB102K	1000p 500V Ceramic	AA
ΔC701	RC-FZ0018CEZZ	0.22 AC250V	AH
ΔC702 | Δ 705, Δ 713	RC-KZ0029CEZZ	0.01 AC250V Ceramic	AC
ΔC707	RC-EZ0151CEZZ	330 400V Electrolytic	AT
ΔC708	VCQPSC2JA333K	0.033 630V Polypro	AB
ΔC709	VCKYPH3DB561K	560p 2kV Ceramic	AC
ΔC710	RC-KZ0024CEZZ	1000p 2kV Ceramic	AD
ΔC714	VCEAGA2AW106M	10 100V Electrolytic	AC
ΔC716	VCEAGA1HW476M	47 50V Electrolytic	AB
ΔC717	VCCSPA1HL221J	220p 50V Ceramic	AA
ΔC719, Δ 720	RC-KZ0023CEZZ	4700p 2kV Ceramic	AD
ΔC721	VCEAAA1CW226M	22 16V Electrolytic	AB
ΔC722	VCEAGA1HW336M	33 50V Electrolytic	AB
ΔC725	VCQYVA1HA822J	8200p 50V Mylar	AA
ΔC726	VCQYVA1HA103J	0.01 50V Mylar	AA
ΔC727	VCE9AA1HW335M	3.3 50V Electrolytic (N.P.)	AE
C731	VCEAAH2CW107M	100 160V Electrolytic	AE
C734	VCEAAA1EW227M	220 25V Electrolytic	AC
ΔC736	VCKYPH3DB271K	270p 2kV Ceramic	AC
ΔC740	VCCSPA1HL151J	150p 50V Ceramic	AA
ΔC741	VCQYSH1HM102K	1000p 50V Mylar	AA
RESISTORS			
ΔR345	VRG-RF2HB3R3K	3.3 1/2W Fuse Resistor	AB
ΔR701, Δ 702	VRD-RA2HD154J	150k 1/2W Carbon	AA
ΔR704	VRG-RF2HB470J	47 1/2W Fuse Resistor	AB
ΔR705	RR-WZ0041CEZZ	0.68 3W Cement	AC
ΔR706	RR-WZ0086CEZZ	0.39 3W Cement	AC
ΔR709	VRS-VV3DB272J	2.7k 2W Metal Oxide	AA
ΔR710	VRG-RF2HB220J	22 1/2W Fuse Resistor	AB
ΔR711, Δ 721	VRD-RA2HD683J	68k 1/2W Carbon	AA
ΔR714	VRD-RA2HD393J	39k 1/2W Carbon	AA
ΔR719, Δ 720	VRC-UA2HG825K	8.2M 1/2W Solid	AA
ΔR722	VRW-KP4AC2R2K	2.2 10W Cement	AD
ΔR723 | Δ 728	VRD-RA2HD823J	82k 1/2W Carbon	AA
ΔR729	VRN-VV3DB1R0J	1 2W Metal Film	AB
ΔR730	VRS-VV3DB271J	270 2W Metal Oxide	AA
ΔR731	VRG-RF2HB2R2K	2.2 1/2W Fuse Resistor	AB
ΔR732	VRD-RA2HD390J	39 1/2W Carbon	AA
ΔR733, Δ 742	VRD-RA2EE102J	1k 1/4W Carbon	AA
ΔR734	VRD-RA2HD223G	22k 1/2W Carbon	AA
ΔR735	VRS-VV3DB333J	33k 2W Metal Oxide	AA
ΔR736	VRS-VV3DB393J	39k 2W Metal Oxide	AA
ΔR739	VRG-RF2EB1R0J	1 1/4W Fuse Resistor	AB
ΔR741	VRD-RA2HD470J	47 1/2W Carbon	AA
ΔR743	VRD-RA2EE681J	680 1/4W Carbon	AA
ΔR744, Δ 745	VRD-RA2HD181J	180 1/2W Carbon	AA
ΔR747	RR-WZ0015CEZZ	2.2 10W Cement	AE
MISCELLANEOUS			
ΔFB701, Δ 703, Δ 704	RBLN-0037CEZZ	Ferrite Bead	AB
ΔFB702	RBLN-0010CEZZ	Ferrite Bead	AC
ΔFB705, Δ 706	RBLN-0036CEZZ	Ferrite Bead	AB

PWB-E DUNTK4717DE01

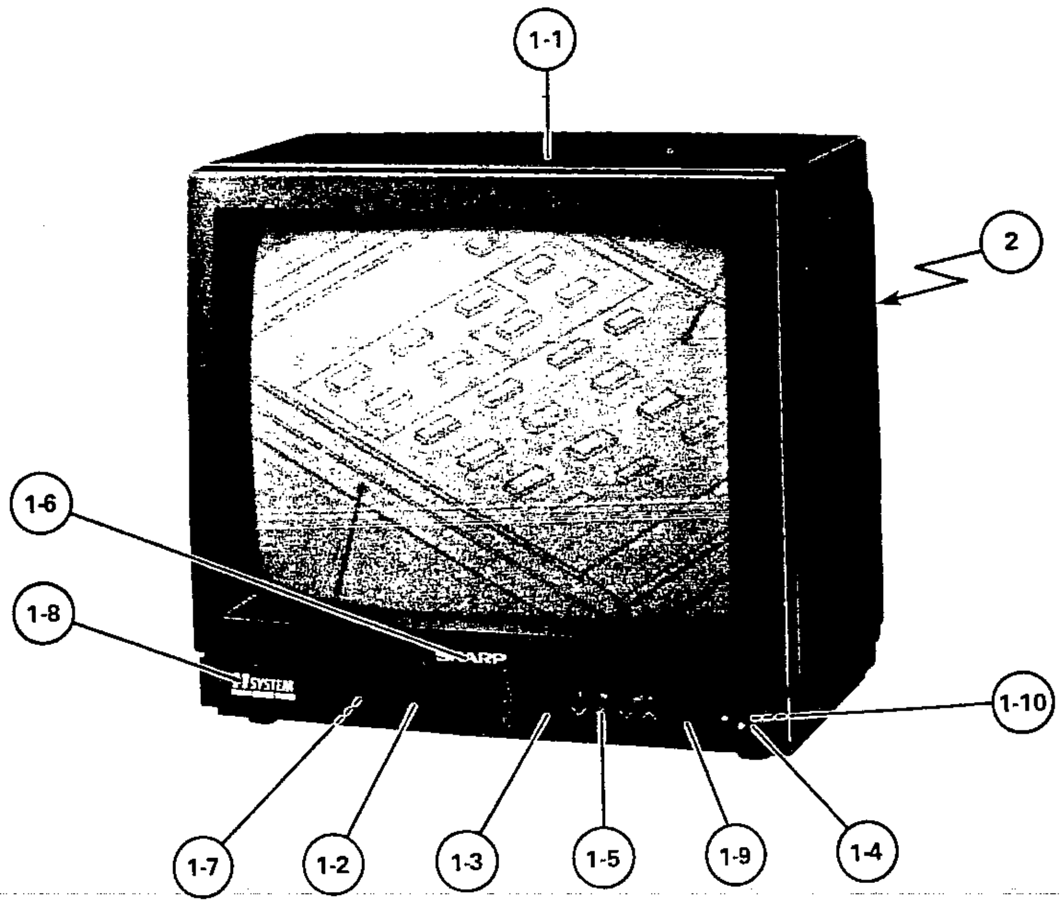
Ref. No.	Part No.	Description	Code
CONTROLS			
ΔR837	RVR-A4061CEZZ	10k(A) Tint	AD
SWITCH			
ΔS801	QSW-S0078CEZZ	Colour System Switch	AH

PWM-A DUNTK4395DE05

Ref. No.	Part No.	Description	Code
INTEGRATED CIRCUIT			
IC931	RH-iX0226CEZZ		AV
TRANSISTOR			
Q936	VS2SC1815GW1E	2SC1815(GW)	AB

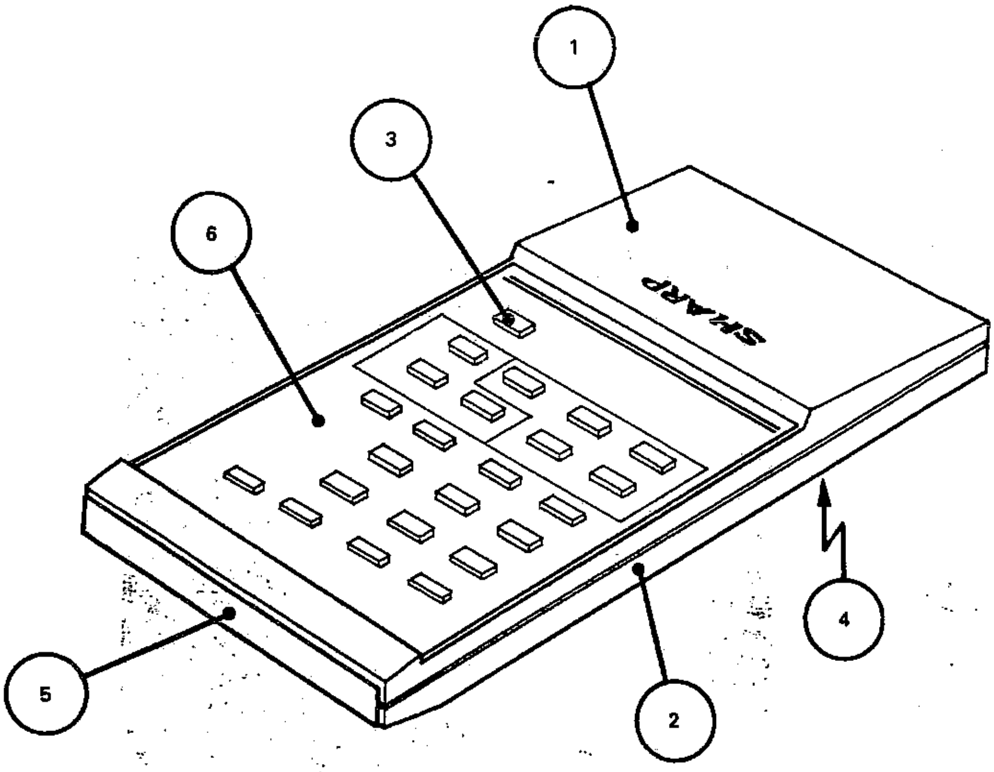
Ref. No.	Part No.	Description	Code
DIODES			
D933, 934, 935, 937	RH-DX0179CEZZ	1SS177	AA
D938	RH-DX0005GEZZ		AA
PACKAGED CIRCUITS			
M931	RMPTC0094CEZZ		AD
M932	RMPTA0063CEZZ		AC
TRANSFORMERS			
T931	RCiLi0364CEZZ		AD
T932, 933	RCiLi0435CEZZ		AE
T934	RCiLi0436CEZZ		AE
CAPACITORS			
C940	RC-KZ0056CEZZ	0.1 16V Ceramic	AB
C944	VCEAGA1CW337M	330 16V Electrolytic	AC
C953, 954, 955	VCSATA1VE105K	1 35V Tantalum	AD

Ref. No.	Part No.	Description	Code
MISCELLANEOUS PARTS			
△	QACCZ3015CEZZ	AC Cord	AM
△	QPLGA0002GEZZ	AC Plug	AK
	QANTR0060CEZZ	Rod Antenna	AU
	RRMCG0372CESB	Remote Control Transmitter	BA
	VSP0080P-B78A	Speaker	AQ
CABINET PARTS			
1	CCABA1634CE01	Front Cabinet Ass'y	BG
1-1	Not Available	Front Cabinet	—
1-2	GDoRF1590CESA	Door	AG
1-3	HDECQ0275CESA	Control Indicator	AF
1-4	JBTN-1347CESE	Power Button	AF
1-5	JBTN-1348CESB	Channel/Volume Button	AE
1-6	HBDGB1057AFSB	"SHARP" Badge	AC
1-7	HiNDM2498CESA	Indicator (Inside Door)	AD
1-8	HBDGS3086CESA	"11 SYSTEM" Badge	AE
1-9	GCoVA1043GESA	LED Cover	AC
1-10	MSPRC0068CEFW	Spring	AA
2	GCABB1633CEKA	Rear Cabinet	AA

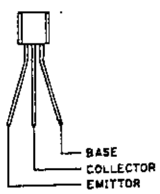


Ref. No.	Part No.	Description	Code
RRMCG0372CESB R/C TRANSMITTER			
INTEGRATED CIRCUIT			
I3001	RH-iX0478PAZZ	LR3714M	AM
TRANSISTORS			
Q3001	VS2SC1815Y/1E	2SC1815Y	AB
Q3002	VS2SC2120Y/-A	2SC2120Y	AC
DIODE			
D3001	RH-PX0068PAZZ	GL521	AD
CERAMIC FILTER			
CF3001	RFiLF0010PAZZ	KBR455BTL	AE

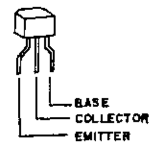
Ref. No.	Part No.	Description	Code
TERMINALS			
	QTANZ0142PAZZ	Battery Terminal (+)	AB
	QTANZ0143PAZZ	Battery Terminal (−)	AB
	QTANZ0138PAZZ	Battery Terminal (+), (−)	AB
CABINET PARTS			
1	GCABA0075AASA	Cabinet−Top	AK
2	GCABB0057AASA	Cabinet−Rear	AD
3	MSPRP0258PASA	Rubber Key	AG
4	GCOVH0049PASA	Battery Cover	AB
5	PFiLW0096PASA	Osc. Filter	AB
6	HPNLH0325PASA	Indication Plate	AE



SOLID STATE DEVICE BASE DIAGRAMS



2SC1815(GW)
2SC1906
2SC1015(Y)
2SC383
2SA1015(GW)
2SC3279
2SC3279N



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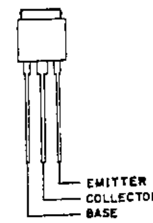
2SC3402



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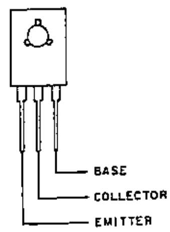

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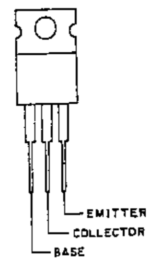

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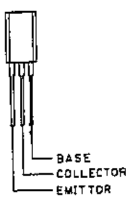

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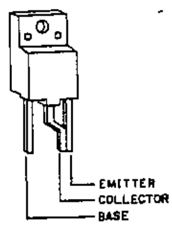
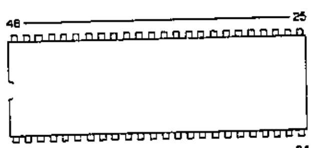


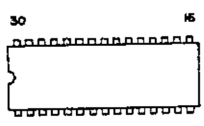
2SD1554

TOP VIEW

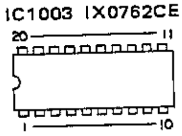
IC801 IX0393CE



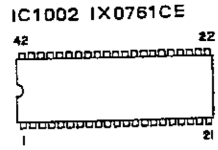
IC931 IX0226CE
IC1801 IX0354CE



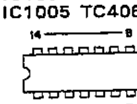
IC1003 IX0762CE



IC1002 IX0761CE

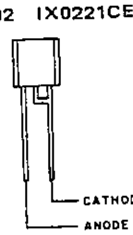


IC1004 IX0378CE
IC1005 TC4066BP

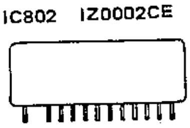


SIDE VIEW

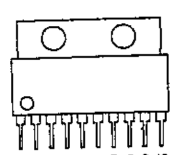
IC702 IX0221CE



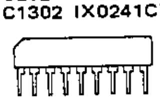
IC802 IZ0002CE



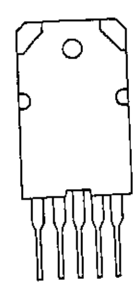
IC1301 IX0250CE



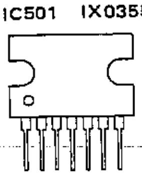
IC202 IX0260CE
IC1302 IX0241CE



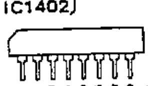
IC701 IX0810CE



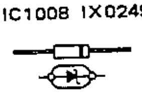
IC501 IX0355CE



IC1001 IX0614CE
IC1303, IC1401, IC1402 LA7016//



IC1008 IX0249CE



IC1006, IC1007 PST520C2